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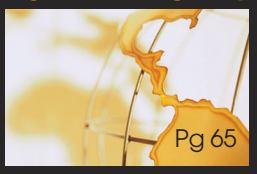
GLOBAL REPORT 3



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The TAS5261, the newest offering in TI's PurePath Digital™ product line, is the highest power single-chip Class D power stage and delivers 110dB SNR for ultimate sound clarity and performance in home audio applications. It drives >300W into a 4Ω speaker (10% THD+N) with 95% efficiency for cooler operation and can drive 125W, 8Ω (THD+N<0.09%).

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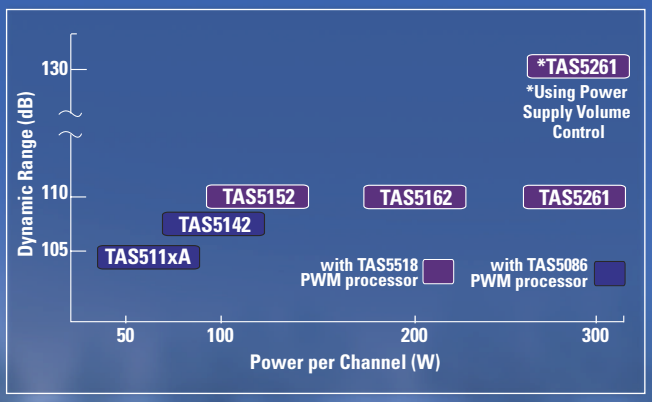

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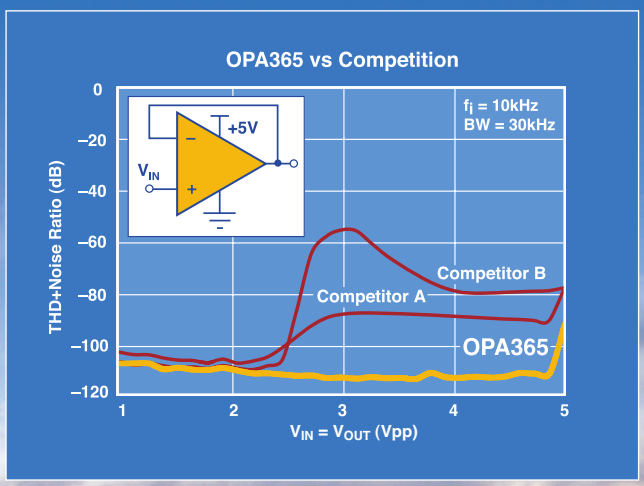

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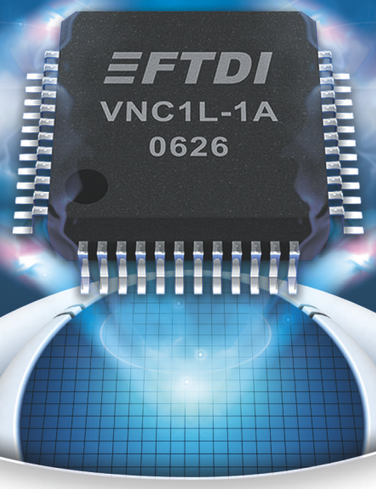


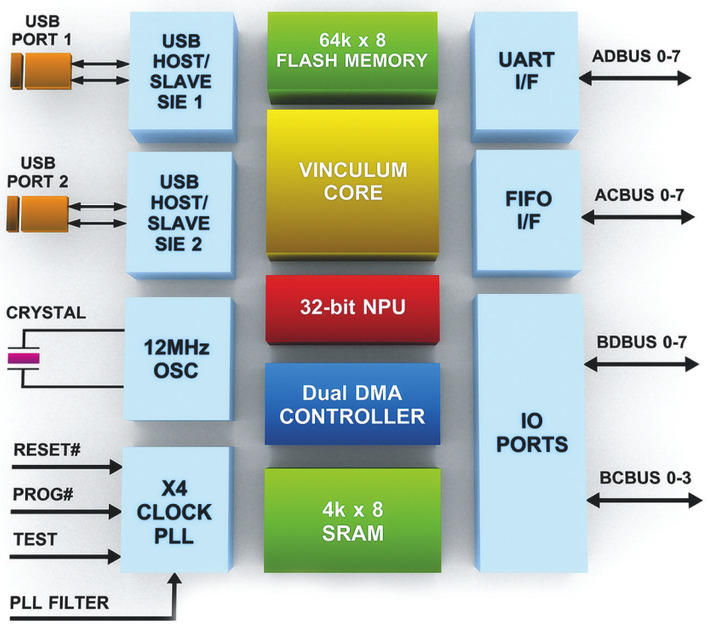
VINCULUM
BINDING USB TECHNOLOGIES

FTDI Chip

The **Vinculum** family of USB Host Controller not only handles the USB Host interface and data transfer functions, but owing to the inbuilt processor core and embedded Flash memory, Vinculum encapsulates the USB device classes as well. When interfacing to mass storage devices such as USB Flash drive, digital camera, or PDA, Vinculum also transparently handles the FAT File structure communicating via UART, SPI or parallel FIFO interfaces via a simple to implement command set. Vinculum provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available.

CONNECTS

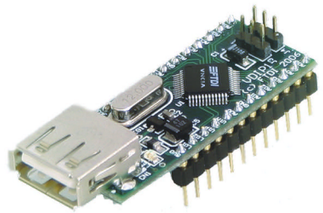
- USB Drive
- Camera
- PDA
- Mobile Phone



WITH

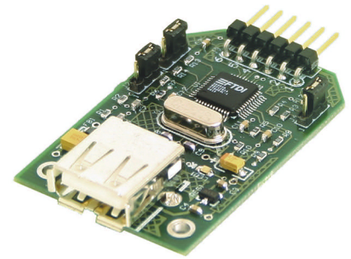
- MCU
- Serial Port
- USB Drive
- Kbd/Mouse

Vinculum Evaluation Modules & Application Areas



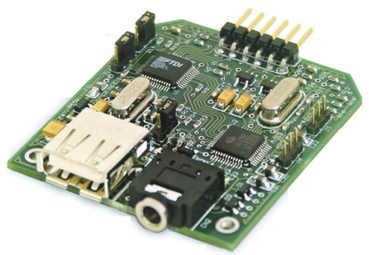
The **VDIP1** module is an MCU to USB Host Controller development module for the VNC1L device and is ideal for rapid prototyping and development of VNC1L designs.

- Jumper selectable UART, SPI or FIFO MCU Interfaces
- USB "A" type socket to interface with USB peripherals
- 2nd USB Interface available via module pins if required
- Single 5V supply input
- Auxiliary 3.3V/200mA power output to power external logic
- Traffic Indicator LEDs



VDRIVE1 is possibly the easiest solution for adding a USB Flash Drive interface to existing products. Only four signal lines plus 5V/GND are required to be connected.

- One USB "A" socket to connect to USB Flash Drive
- Link Selectable UART or SPI interface
- Only 4 signals to connect excluding PWR/GND
- Single 5V supply required
- Easy to implement command set



VMUSIC1 is a product that not only lets you add USB Flash Drive interfacing to your product but allows you to play back MP3 and other popular digital music formats direct from a USB Flash Drive.

- One USB "A" socket to connect to USB Flash Drive
- Stereo 3.5mm headphone jack socket and audio line-out connector for audio playback.
- Link Selectable UART or SPI interface
- Only 4 signals to connect excluding PWR/GND
- Single 5V supply required
- Easy to implement command set

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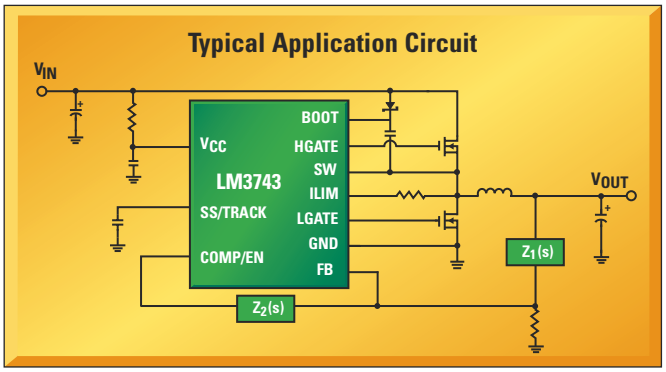

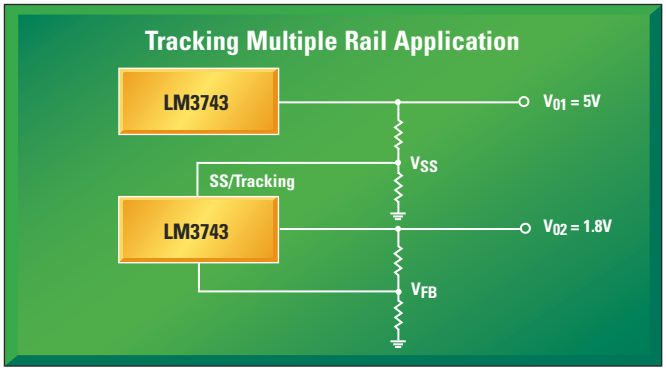

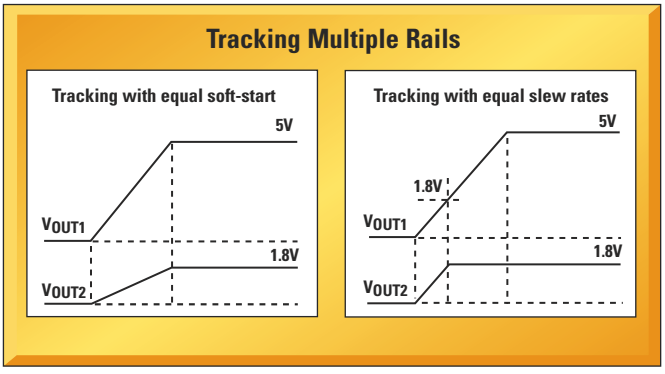

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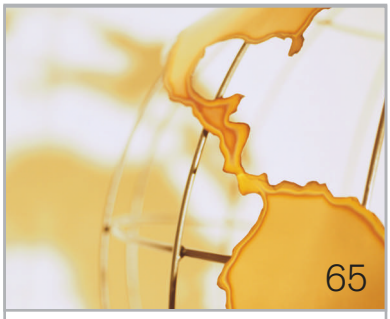


Global Report

Embedded platforms: a second look

 Processing platforms and their software-development ecosystems are becoming more important for the success of designing increasingly complex applications.

by Robert Cravotta, Technical Editor

Consumer electronics: feeling the squeeze

 Designers in the consumer market work under enormous pressures. Have these circumstances changed the way they design chips and systems?

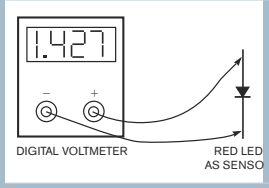
by Ron Wilson, Executive Editor

Fixed-point-IIR-filter challenges

 IIR filters can meet highly selective magnitude-frequency-response specifications with a low-order approach. As such, an IIR is often the technology of choice in realizing frequency-selective tone detectors, narrowband spectral filters, noise rejecters, and digital controllers. Their design, however, entails some unique challenges.

by Michael Christensen, University of Florida, and Fred J Taylor, University of Florida and The Athena Group Inc

DESIGNIDEAS



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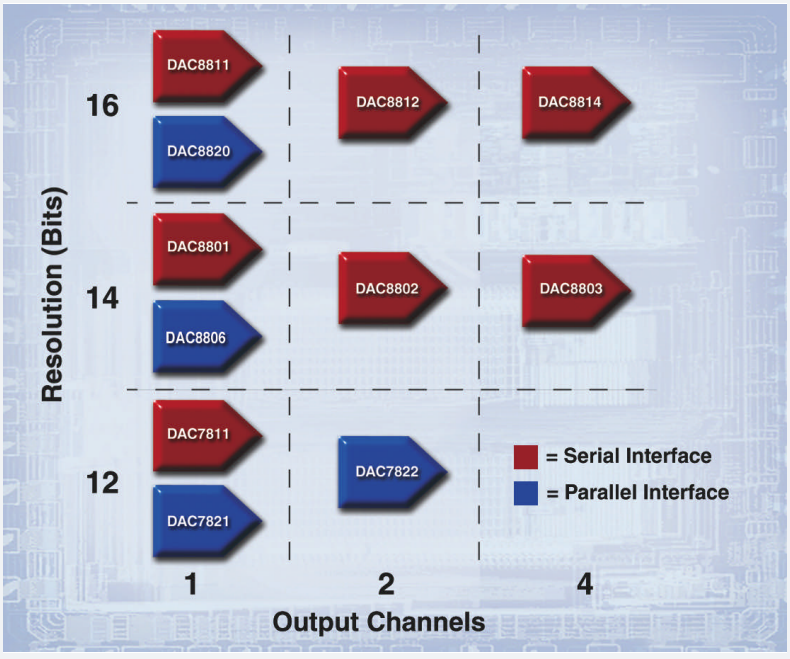
Upgrade Your DAC Designs

Multiplying D/A Converter Family



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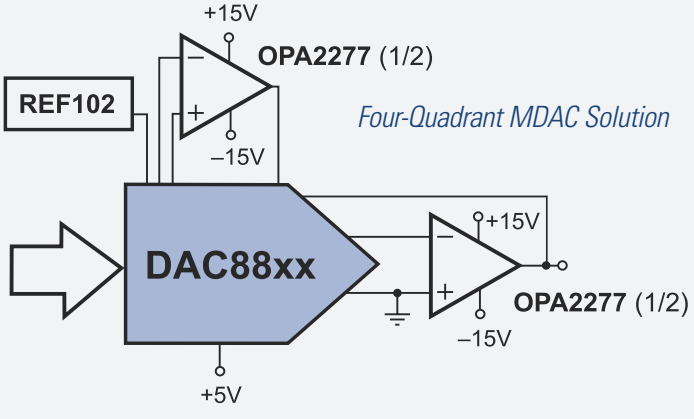
- Pricing in 1k units (starts at):
  - 12-bit: $2.55
  - 14-bit: $4.60
  - 16-bit: $7.15



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pulse


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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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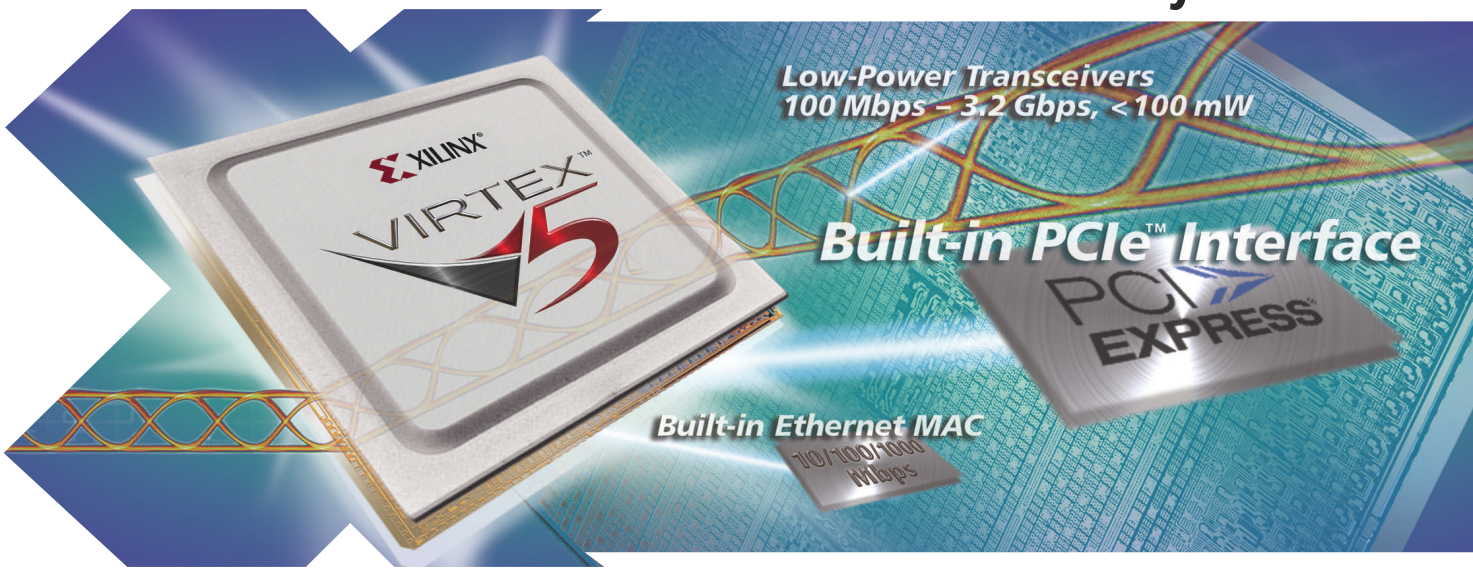

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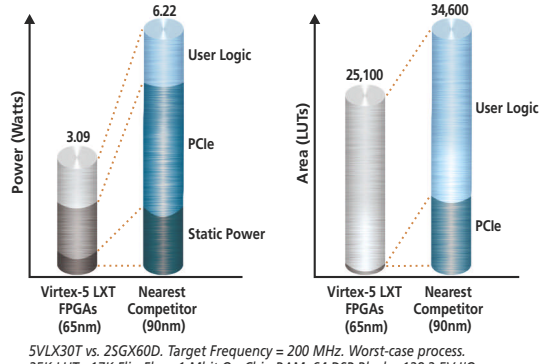

5VLX30T vs. 2SGX60D. Target Frequency = 200 MHz. Worst-case process. 25K LUTs, 17K Flip-Flops,1 Mbit On-Chip RAM, 64 DSP Blocks, 128 2.5V I/Os. Based on Xilinx tool v8.2 and competitor tool v6.0.1

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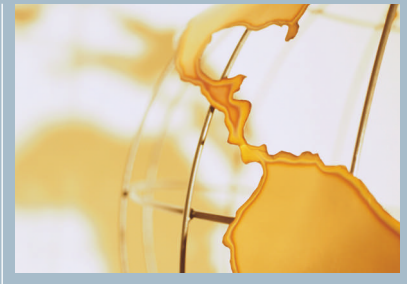

GLOBAL REPORT ONLINE

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INNOVATION NOMINATIONS

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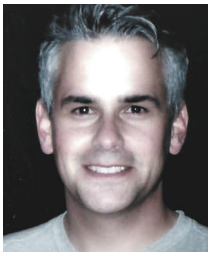


BY MICHAEL SANTARINI, SENIOR EDITOR

EDAC's statistics

Early this year, I wrote a column that raised a few hairs over at the EDAC (EDA Consortium, **Reference 1**). I addressed what I considered a low point for the EDA industry when, in the third quarter of last year, EDAC's MSS (market-statistics services) broadened the definition of EDA to include IP (intellectual property) to make EDA-industry numbers appear better than they were. The semiconductor industry was well into its recovery from the downturn, but this recovery hadn't yet trickled down to the EDA industry. Adding previously unrecorded IP revenue to EDA revenue allowed MSS to keep the EDA industry out of the red for the quarter.

About two quarters later, the traditional EDA-software business legitimately began to grow, even without the help of additional IP revenue. In late September, EDAC announced what appear to be great numbers, indicating that the EDA industry is back on track.

So, now it's time for EDAC to quietly lose the IP-is-EDA stuff—perhaps make IP a separate report or help the IP market create its own industry group. Failing those measures, MSS needs to apply the same statistical standards to design services as it does to IP, so folks can believe in the numbers again.

Statistics is the poetry of mathematics: It's open to broad interpretation and, in the words of poet Wallace Stevens, it "need not have meaning." Indeed, reporting on EDA for the last decade, I've seen some creative studies.

After I criticized MSS's IP push, EDAC retorted with the argument that when it added the current IP revenue to the traditional EDA revenue, it also added the historical revenue from those IP companies to historical EDA revenue, so no deception occurred. Then, at DAC (Design Automation Conference) in July, I found a new angle to the story—something interesting about the statistical sample MSS uses. MSS now includes historic and current revenue in its reports from IP companies that aren't even members of EDAC. Two of the biggest IP vendors, in fact—ARM (www.arm.com) and Rambus (www.rambus.com)—aren't EDAC members and, at last report, *refuse* to be EDAC members, despite the fact that membership would get them a discount on DAC-booth space and would likely get their chief executive officers on more industry panels and in front of members of the trade press, business press, and financial corps. The main reason those two vendors don't join EDAC and don't consider themselves EDA vendors is simple: They are not EDA companies, and they don't want to be lumped into what most consider at best to be a slow but steady growth industry.

But, given that MSS now counts IP vendors as EDA companies and reports revenue even if the IP vendors don't consider themselves EDA companies, why doesn't it apply the same metric for design-services companies? Why doesn't it record revenue from small design houses or pull out revenue from publicly held companies, such as Wipro (www.wipro.com) and Flextronics (www.flextronics.com), which offer IC- and pc-board-design services?

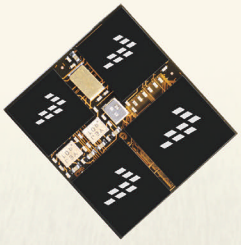
I'll venture a guess. IP has historically shown upward momentum; it's almost a sure bet to grow. Meanwhile, design services has been a volatile segment. We witnessed this volatility years ago, when Cadence (www.cadence.com) executives thought design services was the next big avenue for EDA growth. Cadence's services boomed when things were good and made the industry look great, but when the services business softened, it made the EDA industry look bad, dragging it down even in quarters when traditional software sales were still up. Cadence and the rest of the industry have since pared back their services, so the overall impact of fluctuations on the EDA industry isn't quite as pronounced. But in not applying the same standard to these seemingly equal industries, MSS is being statistically inconsistent; it is cherry picking. With all this statistical creativity, we don't have a truly believable gauge of the industry. We are all left having to read too much into the statistics to glean the truest numbers for the EDA industry.

The EDA industry is already difficult enough to understand for many folks, and EDAC is only making it more difficult. Today, if you want access to the truest account of EDA, you need to become an EDAC member, obtain the raw numbers from EDAC and interpret them yourself, or get a copy of the reports from Merrill Lynch's longtime EDA financial analyst, Jay Vleeschhouwer, who removes the revenue of ARM and Rambus from the MSS quarterly reports to offer investors seemingly the truest historical perspective of EDA. Whichever way you choose, the truth about EDA revenue is hard to obtain, and you'll likely have to pay for it. EDN

REFERENCES

1 Santarini, M, "EDA industry needs a reality check," *EDN*, Jan 19, 2006, pg 16, www.edn.com/article/CA6298273.

You can reach me at michael.santarini@reedbusiness.com.



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The new Virtuoso custom design platform takes precision design to the next level. Now it's all up to you. www.cadence.com/newvirtuoso

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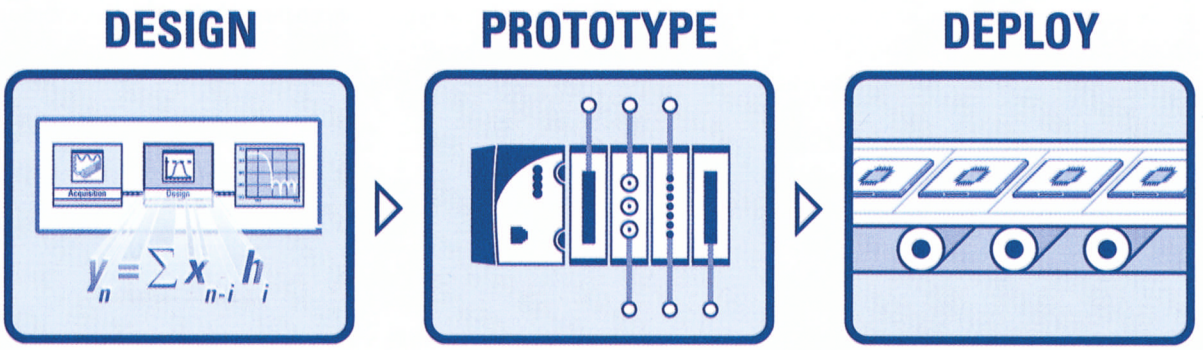
Graphical System Design Delivers 10X Faster Development Time

Graphical system design provides a platform to accelerate the design, prototyping, and deployment of embedded systems.

by Mike Trimborn



Interactive Algorithm Design
- Control design
- Dynamic system simulation
- Digital filter design
- Advanced mathematics

Tight I/O Integration
- I/O modules and drivers
- COTS FPGA hardware
- VHDL and C code integration
- Design validation tools

Deployable Targets
- Rugged deployment platforms
- Distributed networking
- Human-machine interfaces
- Custom designs

Introduction to Graphical System Design

In today's economy, products have to reach the market faster than ever before – relying on more accurate designs; more representative behavioral prototypes; and rugged, reliable deployment devices. However, traditional tools have only delivered incremental improvements over the last decade. The key for achieving an order of magnitude improvement in productivity is to use higher-level tools and abstract lower-level details, while still providing access to low-level component details. Today's system design challenges command a pioneering abstraction platform to deliver nontraditional improvements. According to Mentor Graphics Chairman and CEO Wally Rhines, "Each jump in design-language abstraction has traditionally increased by 10X the number of people that can design ICs."[i] Graphical system design is an approach that can surpass the traditional 10X gain, resulting in 20, 30, or even 50X more engineers, scientists, and domain experts who can design embedded systems.

In addition, with the cost of silicon gates per chip rapidly declining, and with heterogeneous devices containing multiple processors becoming a new reality, there is an increasing focus on software platforms for system design to reduce development costs.[ii]

Although this trend is not new, a search is developing by research and industry for more efficient high-level tools to implement required behaviors, such as:

- Programming parallelism and concurrency, which is critical for FPGAs and devices with multiple CPUs[iii]
- Communication between software and heterogeneous devices
- Heterogeneous model and hybrid system representations of different disciplines in one programming environment
- Multidevice variables and time synchronization

With higher-level tools, such as National Instruments LabVIEW graphical (G) programming software, system-level engineers and domain experts (with little to no embedded expertise) can accurately work with systems of increased complexity and scale, thereby drastically reducing the time from concept to prototype. Thousands of engineers and scientists successfully use G programming as their primary programming tool in a wide range of applications, from design to deployment of machines, remote monitoring systems, embedded systems, ATE systems, and many other complex systems. Graphical programming has surfaced naturally to become a leading tool for system design in a variety of fields.

[i] www.edn.com/article/CA501214.html
[ii] www.freescale.com/files/wireless_comm/doc/brochure/MXCSWDEVWP.pdf
[iii] www-hydra.stanford.edu

NATIONAL INSTRUMENTS

Traditional Design Approach

To better understand the benefits of graphical system design, consider the development process of a device needing customization, such as a motor drive. Using traditional design methodologies, designing this device requires iterating through a variety of steps including hardware design, software design, prototype development, software testing, and system testing and certification. While some of these steps happen in parallel, it is estimated that this entire design cycle takes at least 14 weeks and costs at least $150,000.

This timeline assumes no major setbacks and no future design changes are needed. This forces the engineer or scientist to either build a daughter card to leverage the previous design or abandon the previous design and start from scratch. Regardless of the decision, they are required to go through the 14-week cycle again.

Text-based languages

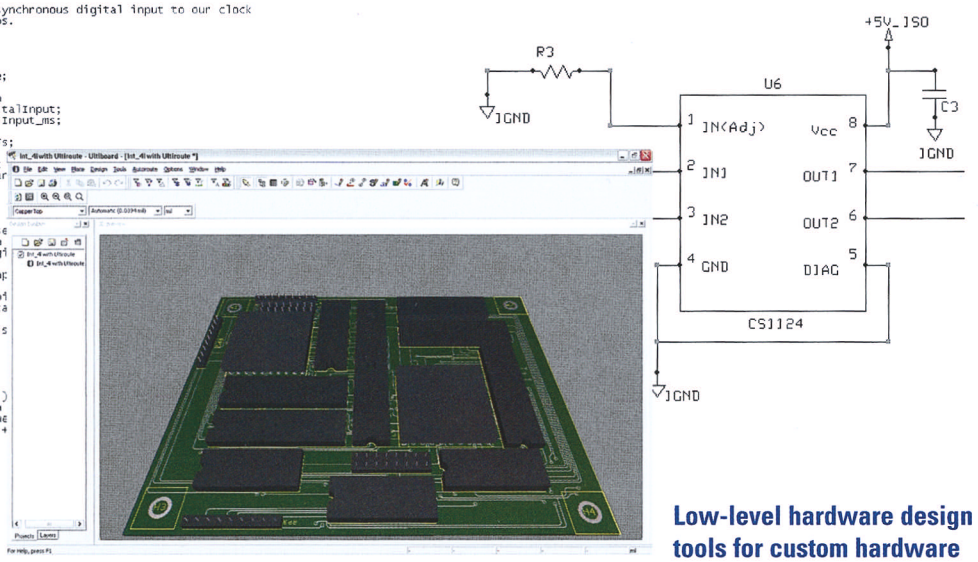
```
-- First we sychronize the asynchronous digital input to our clock
-- by inserting two flip flops.
SynchronizationFFs:
process( aReset, Clk )
begin
  if aReset then
    cDigitalInput_ms <= false;
    cDigitalInput <= false;
  elsif rising_edge(Clk) then
    cDigitalInput_ms <= aDigitalInput;
    cDigitalInput <= cDigitalInput_ms;
  end if;
end process SynchronizationFFs;

-- Then we keep track of what
-- clock cycle by inserting ar
PreviousDigitalInputFF:
process( aReset, Clk )
begin
  if aReset then
    cPrevDigitalInput <= false
  elsif rising_edge(Clk) then
    cPrevDigitalInput <= cDigi
  end if;
end process PreviousDigitalInp

-- Then we have a little combi
cRisingEdgeDetected <= cDigita

-- And finally we have a regis
-- edge is detected.
CounterRegister:
process( aReset, Clk )
begin
  if aReset then
    cCountReg <= (others=>'0')
  elsif rising_edge(Clk) then
    if cRisingEdgeDetected the
      cCountReg <= cCountReg +
    end if;
  end if;
end process CounterRegister;
cCount <= cCountReg;

end rtl;
```



Low-level hardware design tools for custom hardware

- Hardware design .....2 weeks
- First prototype building and testing .....2.5 weeks
- Second prototype building and testing .....1.5 weeks
- Software design and coding .....4 weeks
- Software testing and integration.....2 weeks
- System testing and certification .....2 weeks

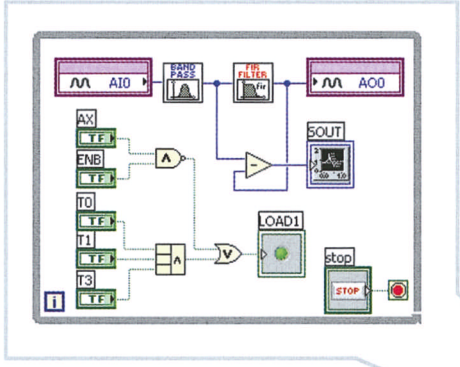
Total: 14 weeks
$150,000

Graphical System Design Approach

Using graphical system design, domain experts can design custom embedded devices such as motion control systems combining flexible, programmable hardware and graphical programming in considerably less time and for less cost, as shown below. Graphical system design uses programmable, commercial off-the-shelf (COTS) real-time processors and reconfigurable FPGAs to provide real-time performance and the customization required in these applications. Using COTS hardware also eliminates time spent working on hardware design, spinning prototypes, and integrating software. Using graphical system design, it is estimated that this entire design cycle takes 4 weeks and costs $15,000 for hardware and software.

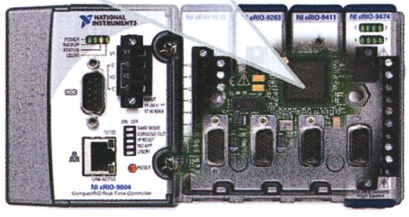
Additionally, graphical programming abstracts the low-level implementations and programming nuances for real-time processors and FPGAs. This not only empowers more engineers and scientists to access the technology, but it also significantly reduces the software development time.

With this software-based approach, end users can focus on the functionality of their systems and less on the low-level implementation. Additionally, as design requirements evolve, implementing changes simply entails updating software or I/O modules.



Graphical languages for FPGAs and real-time processors

Off-the-shelf platform containing microprocessor, FPGA, and rugged I/O



- Hardware design .....0 weeks
- First prototype building and testing .....0 weeks
- Second prototype building and testing .....0 weeks
- Software design and coding .....0.5 weeks
- Software testing and integration .....1.5 weeks
- System testing and certification .....2 weeks

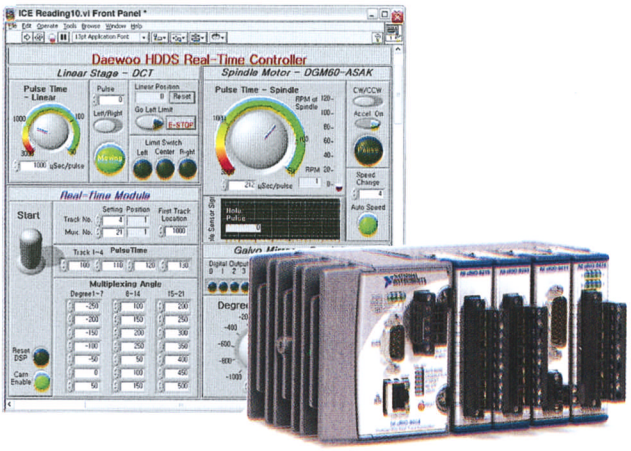
Total: 4 weeks
$15,000

Graphical System Design Applied in the Real World

Consumer Electronics

Daewoo Electronics developed the world's first servo motion control system for three-dimensional holographic digital data storage (HDDS) on continuous rotation disks using NI LabVIEW software and the CompactRIO hardware platform. HDDS technology is one of the most promising new technologies on the horizon for the optical storage industry and promises to accelerate data transfer rates to about one billion bits per second, reduce access times to just tens of microseconds, and increase storage densities toward a theoretical maximum of one trillion bits per cubic centimeter.

The cost estimate of the original solution – using a DSP board – was in the tens of thousands of dollars, with many months required for development. Using flexible LabVIEW software, together with CompactRIO, the company developed its system for only a few thousand dollars without compromising performance. Furthermore, the development period was only one month.

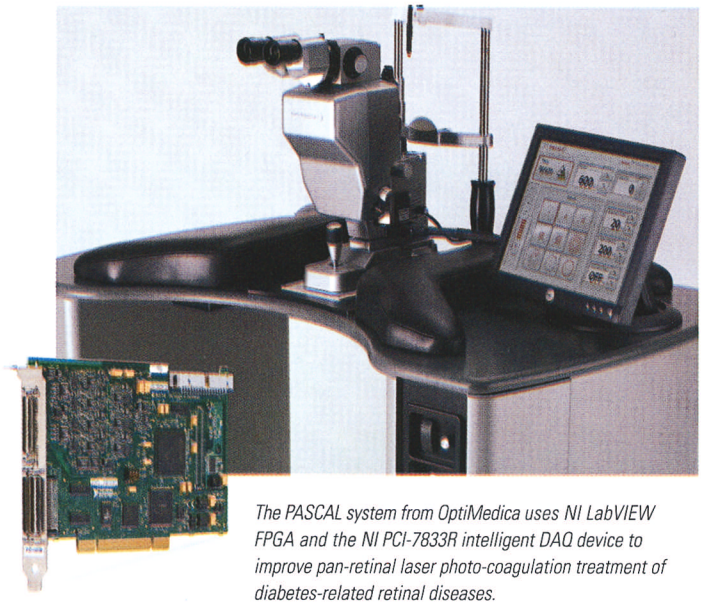


Daewoo Electronics developed a holographic storage device using NI LabVIEW FPGA and CompactRIO.

Medical Devices

Traditional methods of treating retinal diseases caused by diabetes have changed little in the past 35 years. Laser photocoagulation involves the controlled destruction of the peripheral retina using targeted laser pulses. While this treatment has proven highly effective in reducing vision loss, it can be very painful to both patients and doctors. OptiMedica, a company that specializes in designing medical devices that help ophthalmologists improve the way they treat retinal disease, designed the PASCAL photo-coagulator (pattern scan laser) using the LabVIEW FPGA Module and a PCI R Series intelligent data acquisition board.

OptiMedica chose LabVIEW software and R Series hardware over custom hardware because of the ease of development and hardware determinism associated with the FPGA for faster retinal scanning, which significantly reduces the number of office visits for the patient. Using graphical system design, OptiMedica quickly designed, prototyped, and deployed its machine to demonstrate to potential investors. Additionally, using FPGAs provided the reliability of a hardware solution, which does not require the same level of code reviews as processor-based systems when obtaining FDA approval. Finally, by using programmable silicon instead of a fixed ASIC, OptiMedica reduced development time by 30 percent.



The PASCAL system from OptiMedica uses NI LabVIEW FPGA and the NI PCI-7833R intelligent DAQ device to improve pan-retinal laser photo-coagulation treatment of diabetes-related retinal diseases.

To learn how to design faster by viewing Webcasts from National Instruments CEO Dr. James Truchard, Analog Devices, Celoxica, and Maplesoft, visit ni.com/design.

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Reed Electronics Group

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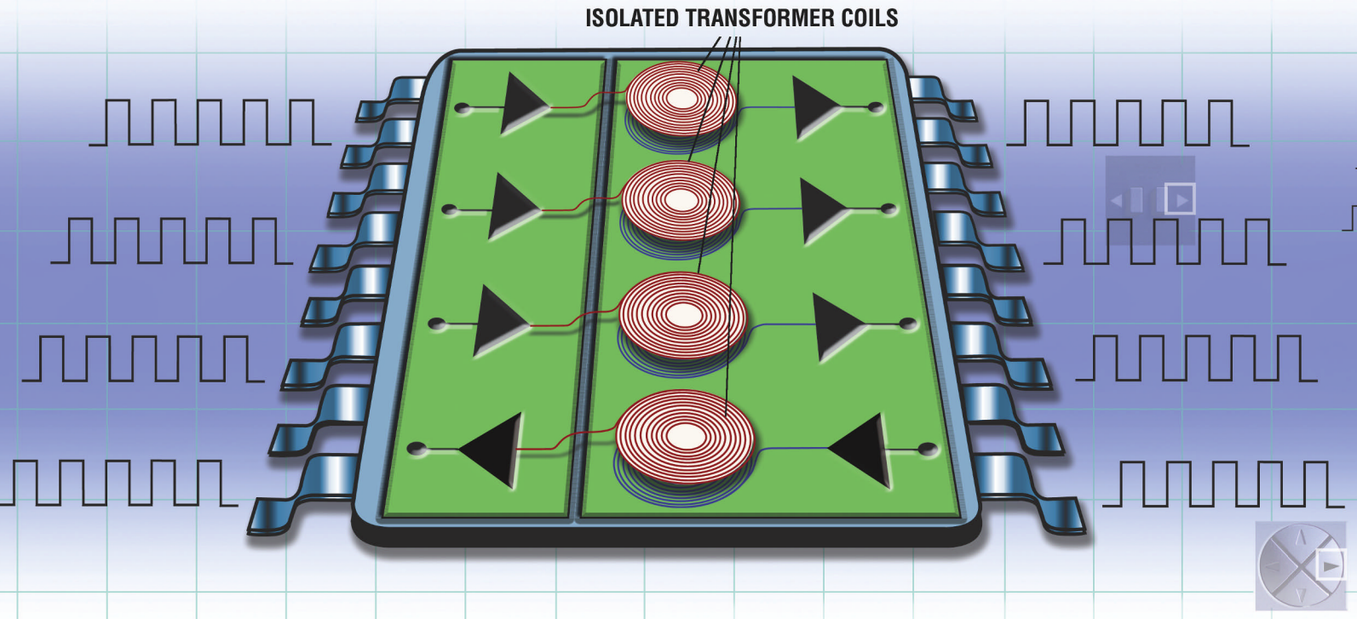
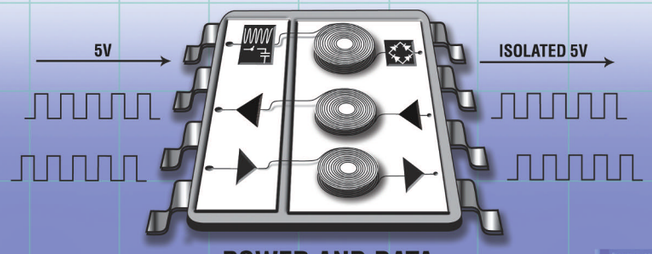
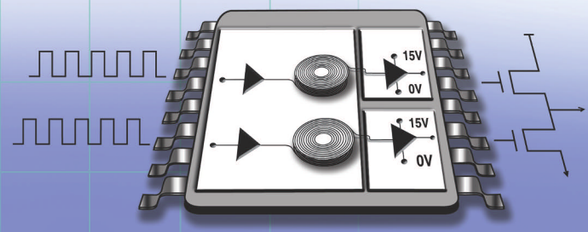


SINGLE AND MULTICHANNEL ISOLATORS

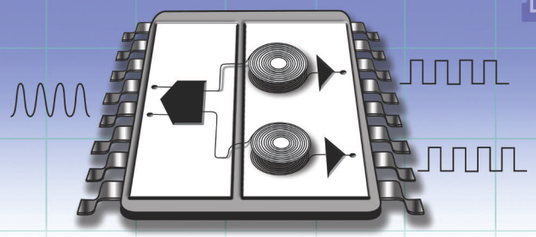
With *i*Coupler, analog is everywhere.



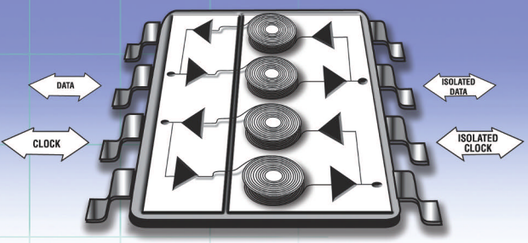
POWER AND DATA



GATE DRIVERS



CONVERTERS



COMMUNICATIONS

Isolating signals, power, and exceptional designs.

*i*Coupler® *digital isolators offer faster data rates, greater reliability, and up to 70% savings in board space and cost, vs. optocoupler solutions.*

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- Variety of input/output channel configurations
- 2.5 kV to 5 kV isolation
- Up to 100 Mbps data rate
- Starting at $0.55/channel

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Industry's first digital isolator with integrated, isolated power

ADuM524x family

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- Variety of input/output channel configurations
- Dual channel, 2.5 kV data isolation
- Starting at $2.95

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Industry's leading converters with integrated isolation

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*i*Coupler technology: Over 75 million isolated channels

*i*Coupler technology represents the state of the art in digital isolation. Unlike common optocoupler isolation techniques, *i*Coupler combines chip scale transformer technology with analog and mixed-signal circuits for significant system level integration, cost savings, and functional advantages. These include:

- Standard isolators that offer faster data rates, greater reliability, and up to 70% savings in board space and cost
- New functionality: bidirectional data paths, combined signal and power isolation, isolation integrated with data converters, I²C, RS-485, and gate driver circuits

Eliminate the performance trade-offs of traditional isolation solutions. See why leading engineers have chosen *i*Coupler technology over optocouplers to isolate more than 75 million channels.

For complete information on *i*Coupler technology, product portfolio, white papers, application notes, samples, and more, please visit our website.

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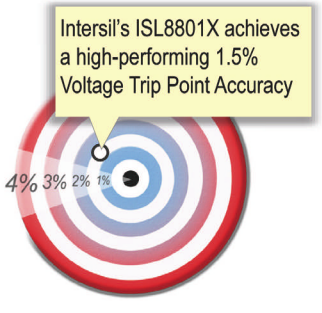
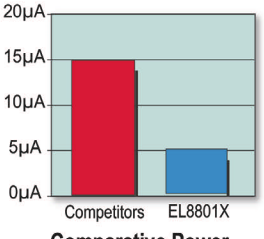
ISL8801X Family's Available Features and Functions	ISL88011	ISL88012	ISL88013	ISL88014	ISL88015
Active-Low Rest ($\overline{RST}$)	●	●	●	●	●
Active-High Rest (RST)	●	●	●		
Watchdog Timer (WDI)			●		●
Dual Voltage Supervision		●			
Adjustable POR Timeout (C_{POR})	●			●	
Manual Reset Input ($\overline{MR}$)	●	●	●	●	●
Fixed Trip Point Voltage	●	●	●		
Adjustable Trip Point Voltage		●		●	●



Voltage Trip Point Accuracy Over Temperature



Comparative Power Consumption

- Small SOT-23 Pb-free package
- Adjustable Power On Reset (POR) timeout delay options
- Watchdog timer with 1.6 sec. Normal and 51 sec Startup timeout durations
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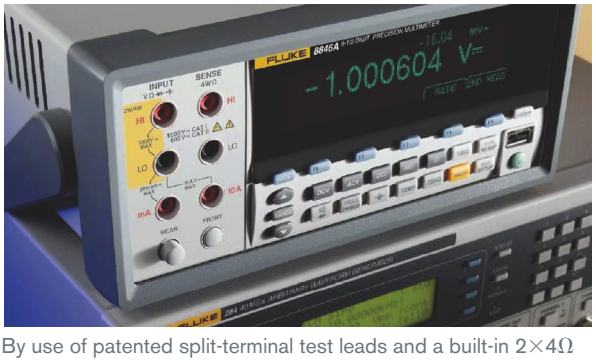
pulse

INNOVATIONS & INNOVATORS

Priced from $995, dual-display benchtop DMMs resolve 6½ digits, make four-wire measurements with two leads

Fluke Corp has announced the 8845A and 8846A Precision DMMs (digital multimeters), which feature 6½-digit resolution, dual displays that show data in graphic or numeric formats, and multifunction-measurement capability. These meters are useful in bench and system applications, including manufacturing test, research and development, and service.

The units perform 14 measurement functions—adding to standard DMM capabilities wider ranges and easy measurement of temperature, capacitance, period, and frequency. The 2×4Ω function uses patented split-terminal jacks that allow users to perform four-wire measurements using only two leads. The meters measure dc voltage with less than 0.0024% error and have a voltage range of 100 mV to 1000V with resolution as fine as 100 nV, a current range of 100 μA to 10A with resolution to 100 pA, and a resistance-measurement range of 10Ω to 1 GΩ with resolution to 10 μΩ.



By use of patented split-terminal test leads and a built-in 2×4Ω function, the 8846A DMM makes four-terminal resistance measurements with only two test leads.

The instruments feature large, bright, dual displays that enable users to measure two parameters of the same signal from one test connection and view the results in graphical or numeric format. Graphical-display modes include TrendPlot paperless chart recording; statistics; and histograms, which enable users to analyze data in real time for efficient troubleshooting of signal-quality issues, such as drift, intermittent malfunctions, and instability.

The meters emulate several legacy benchtop DMMs and feature input terminals on both the front and the rear. Both units include serial, IEEE 488, and Ethernet interfaces and provide multiple drivers to help ensure compatibility with current and emerging standards. The 8846A has a wider feature set, including higher throughput and accuracy, the ability to measure temperature and capacitance, and a USB-device port allowing users to save measurement results to a USB memory stick for later analysis on a PC. The US list prices of the 8845A and 8846A are $995 and $1395, respectively.**—by Dan Strassberg**

▷**Fluke Corp**, www.fluke.com/884XA.

Palm-sized computer features network connectivity

Gumstix's latest miniature computer targets the customized-network-appliance market, and you can use it as a file and print server, a network server, a software-application server, a Web server, an IP (Internet Protocol)-telephony server, or any combination of the these functions. Measuring only 1⅜×4⅛ in., the Netstix 200xm-cf computer combines a 200-MHz Intel (www.intel.com) XScale PXA255-based motherboard with compact flash and 10/100-Gbps Ethernet connectivity. With a Linux operating system, open-source peripheral drivers, and FCC (Federal Communications Commission) Class A certification for business use, the computer becomes a low-cost hardware platform for network-appliance-product development. The basic Netstix 200xm-cf comes with 64 Mbytes of RAM and 16 Mbytes of flash memory, and prices start at $165 (1000).**—by Warren Webb**

▷**Gumstix Inc**, www.gumstix.com.

The Netstix 200xm-cf, a fully functioning, Linux-powered, and network-enabled computer, fits into the palm of your hand.

Tools feed variability data to DFM products

Synopsys has released two new tools to help developers and users of leading-edge processes better predict how proximity variations and global variations will affect circuit performance as the industry moves into 45-nm-IC manufacturing. Terry Ma, director of product marketing for Synopsys' TCAD (technology-computer-aided-design) group, says that, as the industry moves into 45-nm design, process variability will increase. To produce working silicon at that node, foundries are increasing their use of strained silicon. But the process reduction inherently adds more process variability, and the use of new materials further changes transistor characteristics.

To address these issues, Synopsys has added the Seismos and Paramos tools to its Process Aware DFM (design-for-manufacturing) lineup. "Seismos and Paramos will help customers optimize their layouts and realize the full potential of technology scaling, because, if you include too many guardbands, you sacrifice performance," says Ma.

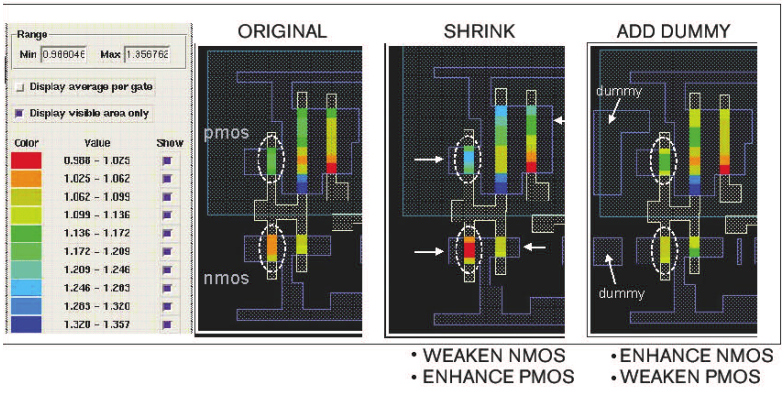
Seismos targets analog-block and full-custom-IC designers, as well as cell and library developers. The tool allows them to analyze how proximity variations arising from stress and well effects will impact transistor characteristics. Users will input a GDSII (Graphic Design System II) layout of their circuit into Seismos and then feed the tool a given foundry line's technology file, stress-parameter file, and command file. The tool then generates a 2-D view of a circuit's layout showing transistor-stress-state characteristics in the current layout. Users can perform what-if analysis on their circuits and, for example, adjust their layouts to see what happens to transistor or circuit performance when they add or subtract dummy fill in proximity to a transistor or group of transistors. For example, users may find that, if they add or eliminate fill in a certain area of their layouts, they can eke out a bit more performance from nearby transistors. The tool handles layouts with millions of transistors and generates an annotated Spice netlist for further detailed simulation with HSpice or a similar simulator.

> The tool handles layouts with millions of transistors and generates an annotated Spice netlist for further detailed simulation with HSpice or a similar simulator.

Foundries and process developers will use Paramos to better characterize global variability for a given process, but the data that Paramos generates will help fabs provide global variability data for Synopsys' DFM tools, including PrimeYield, the PrimeTime VX statistical-timer tool, and the StarRCXT VX extraction tool. Paramos links Spice models directly to manufacturing conditions and extracts process-aware, compact Spice models that combine calibrated TCAD simulations with global Spice extraction. Users can then run a Spice simulation to assess the impact of statistical or systematic process variability on the circuit's performance. TCAD developers can then generate a variation model for statistical-timing simulations of circuit performance, allowing them to explore designs' sensitivity to real physical process parameters. Prices for Seismos start at $150,000 for an annual subscription, and prices for Paramos start at $75,000 for a one-year license.

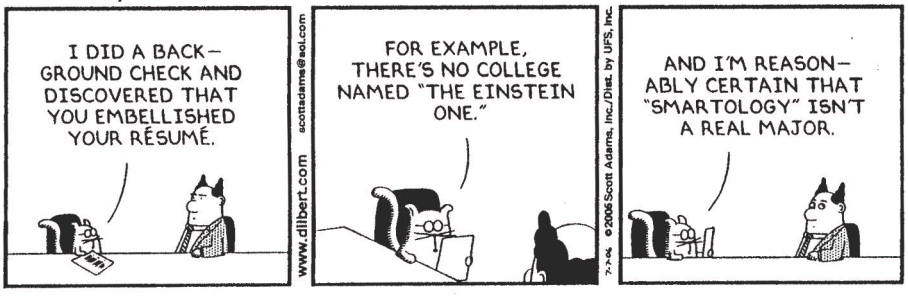
—by Michael Santarini

▷**Synopsys**, www.synopsys.com.



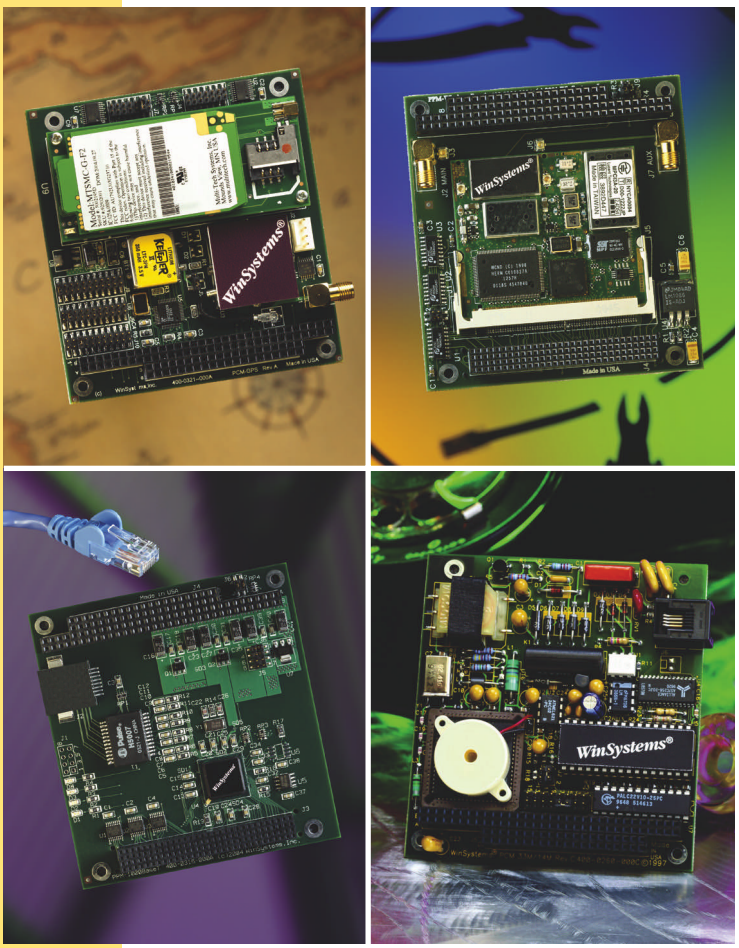
Seismos allows analog-block and full-custom-IC designers, as well as cell and library developers, to analyze how proximity variations from stress and well effects will impact transistor characteristics.

DILBERT By Scott Adams



PC/104 Embedded Machine to Machine Connectivity

Keep in touch with your industrial application by using WinSystems' wired and wireless modular PC/104 modules. Small, rugged, and operational over extended temperature ranges, they are perfect for transportation, pipeline, instrumentation, MIL/COTS, and homeland security applications.



- Wireless
  - GSM/CDMA Cellular
  - 802.11 a/b/g Networking
- Ethernet
  - 10/100 Mbps Ethernet
  - Gigabit Ethernet
- Modem (POTS)
- USB 2.0
- RS-232/422/485 Serial I/O
- Other I/O Expansion
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  - Digital
  - GPS
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  - EPIC – 4.5 x 6.5 inches
  - STD Bus – 4.5 x 6.5 inches
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PIC18 processor includes full Ethernet support

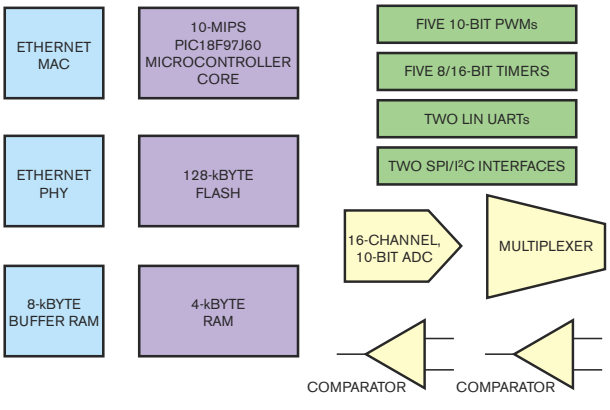
Microchip's PIC18F97J60 family of processors reduces the board space and bill-of-materials costs for 8-bit embedded-system applications needing Ethernet connectivity by eliminating the need for extra chips for the Ethernet MAC (media-access-control) and PHY (physical) layers. This family of 8-bit microcontrollers includes a complete IEEE 802.3-compliant Ethernet controller that comprises a MAC, a PHY, an 8-kbyte transmitter/receiver-RAM buffer, and a free TCP/IP (Transfer Control Protocol/Internet Protocol) software stack in a single package. The nine members of the processor family target industrial and building automation, as well as commercial and home-control applications. The PIC18F97J60 devices are available now at prices starting at $4.24 (10,000) in eight-, 64-, and 100-pin ROHS (reduction-of-hazardous-substances)-compliant TQFPs.

In addition to the PIC18 microcontroller core and on-chip 10BaseT MAC and PHY with an Ethernet buffer, key features of these devices include 128 kbytes of flash; 4 kbytes of SRAM; a 16-channel, 10-bit ADC; five 10-bit PWMs; two comparators; two LIN (local-interconnect-network) UARTs; and two I²C/SPI peripherals. The Ethernet controller supports programmable pattern-match, filtering, and wake-up. These devices are available for the industrial-temperature range of −40 to +85°C. They support seamless migration to add Ethernet support to PIC18 designs.

The TCP/IP stack, a royalty-free, no-cost license, is portable to all PIC18 microcontrollers, and it is available as a download from Microchip. It has a code footprint of approximately 25 kbytes, and the MPLab C18 and Hi-Tech compilers from Microchip and Hi-Tech Software (www.htsoft.com), respectively, support the stack. Microchip offers the AN833 and AN870 application notes for the TCP/IP stack and SNMP (Simple Network Management Protocol) agent, respectively. The PIC18F97J60 PICdem.net 2 demonstration board (DM163024) is available now for $165. The demonstration board enables developers to evaluate the new PIC18F97J60 devices as well as the discrete-component configuration of a PIC18 microcontroller with the ENC28J60 Ethernet controller.

—by Robert Cravotta

▷**Microchip**, www.microchip.com.



The PIC18F97J60 on-chip Ethernet support includes an integrated Ethernet MAC and PHY, along with a dedicated 8-kbyte Ethernet buffer.

SPICE SIMULATOR OFFERS SPEED, CAPACITY INCREASE OVER COMPETITORS

Magma Design Automation is again tapping into its recent acquisition of ACAD to add the FineSim Spice analog tool to its largely digital-tool portfolio. Magma offers the stand-alone, Spice-level circuit simulator with a parallel-computing option. Suk Lee, general manager of the custom-design business unit at Magma, claims that the tool offers comparable accuracy with market-leading Spice simulators but is three to five times faster and has larger capacity. "FineSim Spice's parallel capability allows users to simulate a circuit with much faster linear scalability and handle a larger circuit than was possible before," says Lee.

The release of FineSim Spice follows the July release of FineSim Pro, a trimode circuit simulator, which has one mode that offers similar capabilities to those of FineSim Spice. "FineSim Pro allows designers to use different modes, depending on their speed-versus-accuracy requirements," says Lee. FineSim Spice accepts any standard inputs, such as Spice netlists, including back-annotated RLC (resistance/inductance/capacitance) information in DSPF (detailed-standard-parasitic-format), model-netlist, and stimulus-vector inputs. The tool then generates various Spice-simulation-standard outputs, such as tr0 files and fsdb files for waveform viewers. The analysis results include measured data, timing information, power consumption, IR-drop-analysis results, and more.—by Michael Santarini

▶**Magma Design Automation,** www.magma-da.com.

11.09.06

FROM THE VAULT

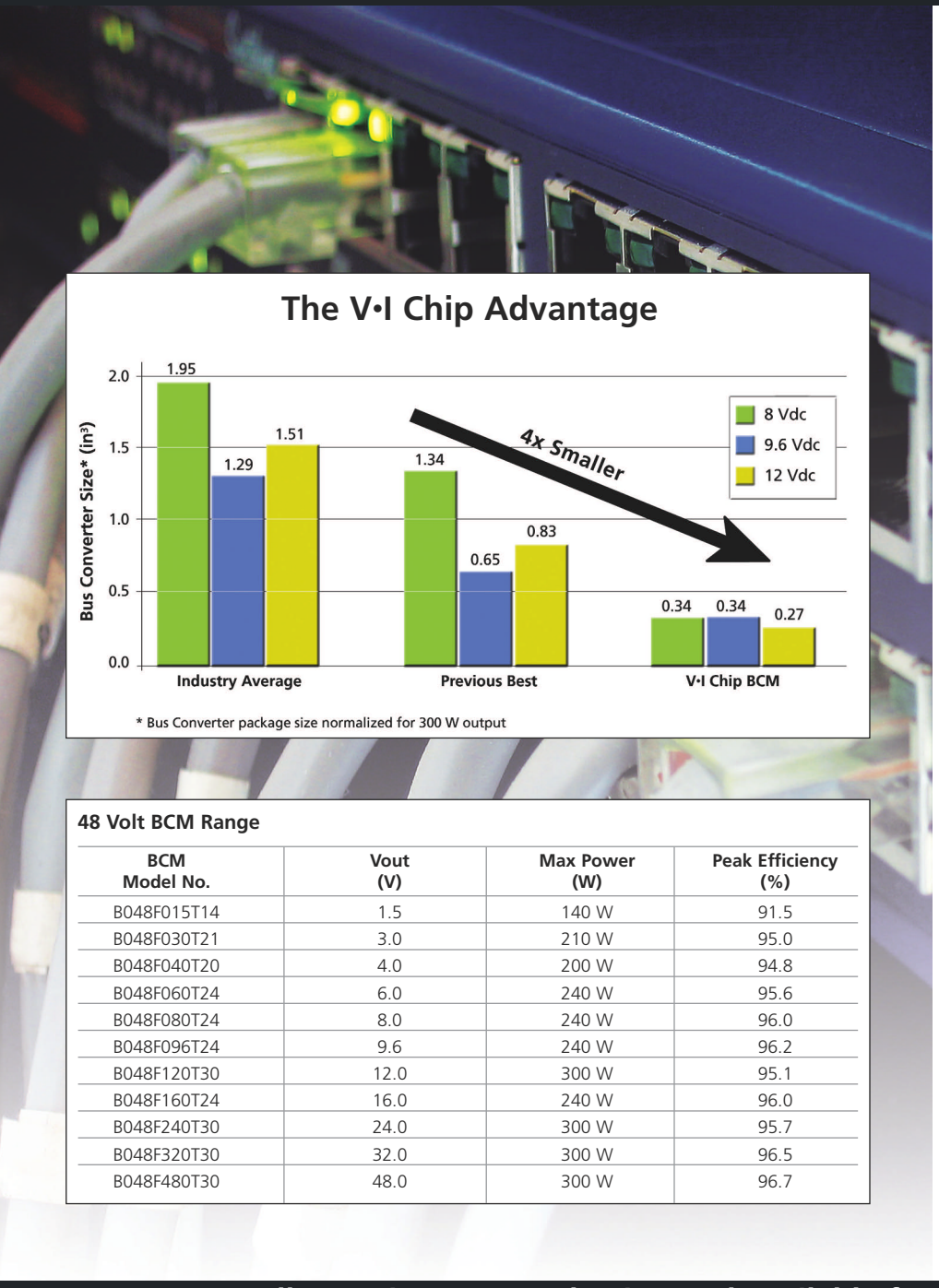
"Improvements in sensor technology and system needs for higher accuracy and throughput are pushing 14- and 16-bit ADCs well into the megahertz region. ... Matching system requirements to the appropriate ADC specifications is crucial because these converters cost at least hundreds and sometimes thousands of dollars."

Anne Watson Swager, Technical Editor, *EDN*, Oct 28, 1993, pg 76

Twice the Power

Half the Size

48 V Bus Converters Increase Port Density and Processing Throughput



The V•I Chip Advantage

* Bus Converter package size normalized for 300 W output

48 Volt BCM Range

BCM Model No.	Vout (V)	Max Power (W)	Peak Efficiency (%)
B048F015T14	1.5	140 W	91.5
B048F030T21	3.0	210 W	95.0
B048F040T20	4.0	200 W	94.8
B048F060T24	6.0	240 W	95.6
B048F080T24	8.0	240 W	96.0
B048F096T24	9.6	240 W	96.2
B048F120T30	12.0	300 W	95.1
B048F160T24	16.0	240 W	96.0
B048F240T30	24.0	300 W	95.7
B048F320T30	32.0	300 W	96.5
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UniVox enables manufacturers to produce wireless phones for residential use at low cost and power with as much as 20 hours of talk time and 400 hours of standby time from typical handset batteries.

GLOBAL DESIGNER

VOIP-phone reference design targets low cost, power

CSR (Cambridge Silicon Radio) based its UniVox VOIP (Voice over Internet Protocol)-phone reference design on the CSR UniFi single-chip Wi-Fi device. UniVox enables manufacturers to produce wireless phones for residential use at low cost and power with as much as 20 hours of talk time and 400 hours of standby time from typical (1500-mAhr) handset batteries, using latest generation access points. CSR provides UniVox customers with schematics, layout, and BOMs (bills of materials), as well as royalty-free design software. The BOM cost is less than $20, and the electronic BOM totals less than $15.

CSR's UniFi-1 802.11b/g single-chip Wi-Fi silicon occupies a chip-scale package with a footprint of 6×6 mm. CSR has also designed its own MAP (multimedia-applications processor) into UniVox, combining a low-power, RISC-based application processor with a DSP function, audio codecs, echo cancellation, and intelligent power management. UniVox supports 802.11e and WMM (Wi-Fi multimedia) to provide optimized and prioritized quality of service, eliminating potential latency or jitter. UniVox also supports 802.11i to add enhanced levels of security, and SIP (Session Initiation Protocol) Version 2, the widely adopted open standard for initiating voice or video calls across Internet connections. Designers can also configure it to support the alternative IAX2 protocol. The DSP coprocessor inside CSR's application processor includes the company's own CVC (Clear Voice Capture) echo-cancellation software.

—by Graham Prophet, *EDN Europe*

▷**CSR,** www.csr.com.

11.09.06

COTS PRINCIPLES SHAPE DC/DC CONVERTERS

XP Power's MTC series of dc/dc-converter modules targets military and avionics applications, following the principles of COTS (commercial-off-the-shelf) and NDI (non-development-item) procurement. Spanning the 4 to 35W power range, the converters accept an input voltage of 15 to 40V, centered on the 28V power bus common in military vehicles. The input range of almost 3-to-1–rather than the 2-to-1 range of commercial units, which often accept 18 to 36V–provides continuous operation through deep transient drops in a vehicle's supply.

A separate filter unit conditions incoming power to handle 100V, 50-msec transients. The units operate at a case temperature of 100°C; the thermal design ensures that semiconductor-device-junction temperatures are only a few degrees higher than the case temperature. XP also guarantees that the units will start at an ambient temperature of −40°C. The design bonds power devices directly to the "cold" plate (base) of the module; the construction employs separate power and control pc boards within a robust extruded housing, and the assembly process includes complete filling of interior spaces with a compound that provides high resistance to g forces.

The MTC series runs at a switching frequency of 450 kHz and employs synchronous rectifications in its 3.3- and 5V-output variants; other voltages are 12, 15, and 28V. System designers can lock the switching operation to synchronize with an external frequency. The fully protected supply has a "battle-mode" option that removes all protection features and allows continued operation in out-of-specification conditions when survival of the power supply is no longer the highest priority. EMC emissions and susceptibility meet all relevant military standards. XP intends the MTC to occupy a market position between standard-commercial and full-custom units, offering medium cost and rapid delivery but with a full military specification; prices range from $150 to $250.—by Graham Prophet, *EDN Europe*

▶**XP Power,** www.xppower.com.

The MTC series of dc/dc-converter modules targets military and avionics applications, spanning the 4 to 35W power range and accepting an input voltage of 15 to 40V, centered on the 28V power bus common in military vehicles.

Blackfin is all eyes

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Multichannel H.264/MPEG4
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The inability to support multiple video standards threatened the life span of Zhejiang Dali's digital video recorders for surveillance systems. Until the Blackfin® Processor entered the picture. With 1200 MMACS and quad 8-bit video ALUs embedded in its dual-core architecture, Blackfin enables Dali's systems to easily process present and future video standards, including H.264 and MPEG4 on 16 channels at D1 resolution. Now Blackfin is everywhere, keeping an eye on things.

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ANALOG DEVICES

RESEARCH UPDATE

BY MATTHEW MILLER

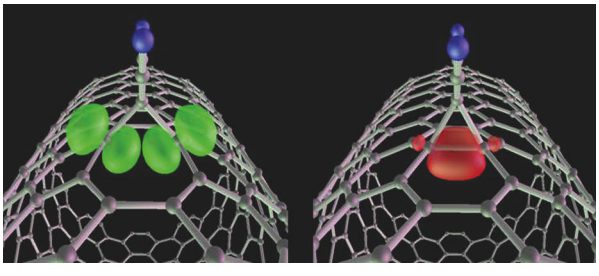
Researchers get a handle on carbon nanotubes

Announcements about carbon nanotubes seem to be nearly as abundant as carbon itself these days, but most gloss over a fundamental challenge: These nanotubes—cylindrical carbon molecules 50,000 times thinner than a human hair—are devilishly difficult to manipulate. Noting that a batch of nanotubes is more likely to resemble a bowl of spaghetti than a circuit or any other useful structure, a group of researchers at the Massachusetts Institute of Technology has developed a way of attaching molecular "handles" to the sides of the nanotubes.

Others have accomplished similar feats, but the MIT team claims that its handles are the first to afford control over nanotubes without reducing their near-perfect conductivity. Like fuzzy balls and Velcro, the hexagon of carbon that makes up a nanotube has a predeliction for clinging to other hexagons. The researchers identified carbenes and nitrenes that not only provide a grip on the nanotubes, but also prevent them from sticking to each other—a serious problem with the gregarious, hexagonal structures.

The MIT scientists also report that some of their handles can transform from a bond-intact to a bond-broken state, which may provide the ability to switch the nanotubes' conductivity on or off in the presence of certain substances or a laser beam. "This direct control of conductance may lead to novel strategies for the manipulation and assembly of nanotubes in metallic interconnects or to sensing or imaging devices that respond in real time to optical or chemical stimuli," says Nicola Mazari, an associate professor in the materials-science and -engineering department at MIT, who, along with Young-Su Lee, a graduate student in the same department, led the study. This method of control may propel nanotubes into useful applications in interconnect, chemical detectors, and image sensors, according to MIT.

▷**Massachusetts Institute of Technology**, www.mit.edu.



Molecular "handles" make carbon nanotubes easier to manipulate and also allow them to switch between highly conductive (left) and poorly conductive (right) states.

Codec compresses in-vehicle imagery

Fujitsu Laboratories has announced SmartCodec, an image-compression technology targeting automotive applications, which would ease the transportation of video entertainment, navigation-system imagery, and real-time video from exterior cameras. Compliant with the IDB (ITS Data Bus)-1394 standard, the codec allows car makers to multiplex multiple video streams on a single 400-Mbps 1394 cable.

The hardware-based technology features a 3-to-1 compression ratio, a compression/decompression time of 2 to 3 msec, and encoding techniques to preserve details such as the fine lines on a navigation-system map display, according to the company. The requisite circuitry fits within an IDB-1394 controller and requires no external memory.

▷**Fujitsu Laboratories**, www.fujitsulabs.com.

11.09.06

LAB PUBLICIZES ANOTHER WI-FI WORRY

Hoping to head off a potential security threat, Sandia National Laboratories has demonstrated a passive technique that unsavory characters could use to identify the device driver in use by an 802.11 radio. The perpetrators could then exploit the information to launch a driver-specific attack.

The technique analyzes the timing of the "probe-request frames" that Wi-Fi cards or modules send out as they scan for access points. Because the 802.11 specifications don't explicitly spell out this part of the implementation, device drivers from different companies use different and, thus, identifiable timing, according to the Sandia researchers.

The lab's "fingerprinting" technique requires only a few minutes' worth of network data and is effective 77 to 96% of the time, depending on the setting, according to the researchers. The team suggests several potential fixes, including standardizing the timing of probe-request frames and introducing noise to mask the true timing. Go to www.edn.com/061109ru for a link to the paper describing the fingerprinting technique.

▶**Sandia National Laboratories,** www.sandia.gov.

Beware: Real Wi-Fi snoops might not make themselves quite as conspicuous as the one in this dramatization.

Blackfin is at 32°54.6 N, 96°45.1 W

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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Eye don't like it

My heart sank when I first saw the hideous jitter and loss of noise margin evident in the eye diagram of **Figure 1**.

The **figure** shows the received eye diagram for a simple serial connection operating at 2.5 Gbps. This differential link connects a fiber-optic receiver module (O/E) to a large protocol processing chip (PHY). The **figure** illustrates the signal measured with a high-bandwidth differential probe at the receiving end of the link (**Figure 2**). Data goes from left to right in the picture.

The layout for this system looks perfect. Both O/E and PHY modules provide easily accessible differential ball pairs at the edges of their respective pin fields. The layout designer wisely chose to keep these short differential traces on the top layer only, avoiding all vias. So why does the eye diagram look so awful? To address that question, you must peel apart the eye diagram.

Every eye diagram comprises many small snippets of the received signal. Your oscilloscope first captures one snippet, then a second, and aligns the timing of the snippets bit for bit before superimposing them. The scope continues accumulating snippets in this way until, finally, it displays portions of every conceivable bit pattern.

In the complete eye diagram, your most troublesome patterns resemble low-hanging fruit within the eye opening, making them easy to spot. What a great way to check margins in a finished system!

Unfortunately, the eye diagram makes a terrible diagnostic tool. It shows aggregate performance but clutters the picture with an overabundance of useless information, making it difficult to determine which edge causes which artifact.

A step-response test straightens out the clutter. This test repeatedly stimulates the system with just one step transition, preceded and followed by the longest contiguous strings of zeros and ones that you can manage. Use vertical averaging during this test to block random noise. The step-response test pinpoints all artifacts resulting from each individual bit transition.

Figure 1 highlights in red the system step response. This step response reveals an initial rising edge followed by a negative blip, possibly a reflection, centered 400 psec after the midpoint of the main edge. An upcoming column investigates some possible causes of that blip. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

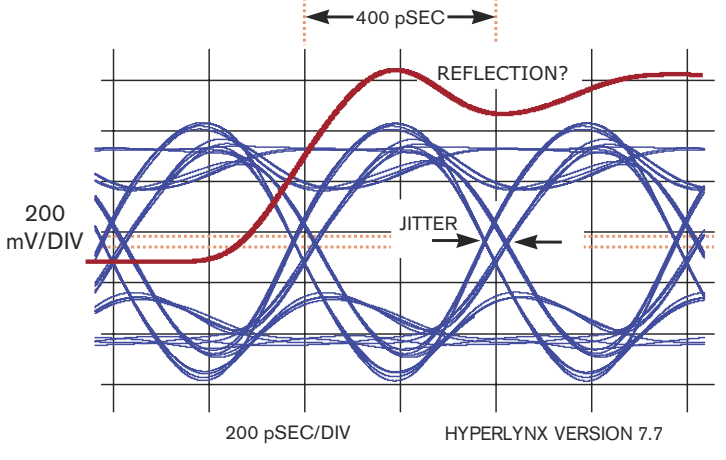


Figure 1 An eye diagram superimposes the responses to many different random bit patterns.

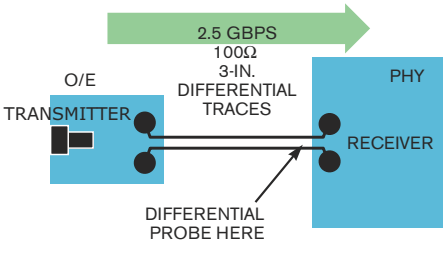
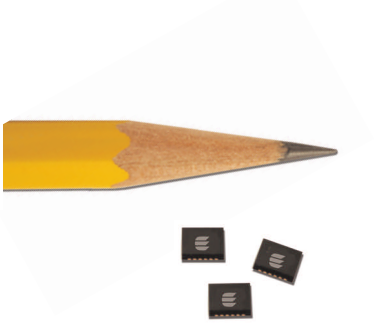


Figure 2 At high speeds, even this simple circuit elicits a complex response.

CONTROL MADE EASY

Need to monitor or control the small sensors and actuators in your control network? Or make your machine more reliable, easy to assemble and remotely accessed? Use Pyxos™, the embedded control networking solution that installs with push-button simplicity. Pyxos chips are small enough for nearly any sensor or actuator, and includes a digital I/O and SPI port to use with existing microcontrollers. It extends the power of LonWorks® control networks to the smallest of devices, plays well with others—host processors and PLCs—and has the development tools and reference designs to reduce your development time.



- ☑ Deterministic TDMA protocol
- ☑ Bit rate: 312.5kbps
- ☑ Scan time for 32 devices: ≤25ms
- ☑ Wire type: 16AWG (1.3mm) to 24AWG cat5 (0.5mm)
- ☑ 24VAC or DC power and data on two wires
- ☑ Application power delivered to each device: 100mA@3.3VDC
- ☑ Built-in unique MAC ID
- ☑ Plug-and-play or preconfigured self-installation
- ☑ 20MLF (5mm x 5mm) RoHS-compliant IC package

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FPGAs entered at PLD density but became integration champ

Today, FPGAs, along with memory chips, are the densest ICs in production. The regular structure of FPGA die makes the chips ideal for pushing the evolution of process technology, and designers seemingly can't get enough equivalent gates. Xilinx's latest Virtex-5 family features chips with as many as 1 billion transistors.

The first FPGA, the Xilinx XC 2064, arrived in 1985, although *EDN* still labeled it a PLD (programmable-logic device) even while acknowledging its gate-array-like architecture. The May 15, 1986, *EDN* article, "Programmable logic devices" (www.edn.com/article/CA6370622), questioned the wisdom of a volatile SRAM-based architecture. But again, Moore's Law prevailed, and the FPGA's simpler manufacturing process, compared with the PLD, became the density champion in the programmable-logic race.

That XC 2064 integrated the equivalent of about 1200 logic gates. Over 20 years, FPGA density has increased by a factor of more than 5000. The Latest Virtex-5 V5LX330T offers about 7 million equivalent gates.

Today, FPGAs span a spectrum of density and applications. Engineers still use the densest devices quite a lot in prototype applications, and those devices are also finding sockets in communication systems that can absorb the relatively high per-chip price. Lower density devices are shipping in some of the highest volume products in the electronics market, such as flat-panel TVs and displays.

The FPGA earned its spot on *EDN*'s Milestones That Mattered time line by enabling the average engineer to become a chip designer. Indeed, easy-to-use software even allows mechanical or software engineers to have access to FPGAs. In "Miniaturization enables innovation—past, present, and future" from *EDN*'s just-published 50th-anniversary edition, Mentor Graphics CEO Wally Rhines lauds the FPGA for just such an accomplishment, noting that because of the FPGA, we'll soon have 5 million IC designers.EDN

05.15.86

FROM THE VAULT

Programmable logic devices

FROM ITS HUMBLE ORIGINS, THE PROGRAMMABLE LOGIC DEVICE HAS EVOLVED INTO A COMPLEX PART WITH THE ABILITY TO IMPLEMENT SEQUENTIAL AND COMBINATORIAL CIRCUITS. CMOS TECHNOLOGY LETS YOU REPROGRAM PLDs AND REDUCE SYSTEM POWER CONSUMPTION; BIPOLAR PLDs CAN HELP INCREASE SYSTEM SPEED.

Advances in programmable logic devices' architectures are making PLDs suitable for a plethora of applications. The devices now find use in state machines and other highly sequential circuits. In the past two years, bipolar PLD operating speeds have doubled, and emerging CMOS PLDs offer four times the circuitry per chip than the older bipolar versions offered. CMOS PLDs also offer lower operating currents, erasability and reprogrammability, and testability that promises close to a 100% yield of working parts.

Only one vendor, Xilinx, has abandoned the PLA-based PLD design altogether in favor of an architecture more like that of a gate array. Xilinx's PLD, the XC 2064, comprises 64 individual blocks of logic in a sea of interconnects. Both the blocks and the interconnects are programmable. Because the circuits you build don't conform to a PLA-like structure, you have more freedom in using registers than you do in the PLA-based devices.

You use the logic in a logic block in a way similar to the manner in which you would define the function of cells in a gate array. Each logic block contains a 4-input logic cell that can implement logic functions. The blocks also contain a register and feedback lines. The XC 2064 can implement as many as 1500 equivalent gates of logic, so you can use it instead of a small gate array, in place of 15 to 75 SSI and MSI ICs, or as substitutes for as many as four PAL devices, according to the vendor.

Most of the companies new to the PLD market are concentrating on CMOS devices, because the technology can yield PLDs that are amenable to more circuit designs than are bipolar PAL devices. The principal advantage of CMOS is that, by virtue of its simpler layout and lower power consumption per unit of silicon area, it can create much more dense and complex circuitry. Also, any CMOS part should have better supply-voltage tolerance and noise margins than corresponding bipolar parts. CMOS vendors list other benefits—lower power consumption in its own right, testability, and erasability—but you should inspect them carefully to determine whether they actually benefit your design.

For example, though CMOS devices generally consume less power than equivalent bipolar devices, at high frequencies they may actually consume the same amount of power, because CMOS power consumption is proportional to operating frequency. Check the power consumption at the frequencies at which you expect your circuit will operate. Quarter- and half-power bipolar devices may consume the same amount of power as some CMOS devices.

—by David Smith, Associate Editor, *EDN*, May 15, 1986

Quick Brief

Low Power FPGA Solutions for Interface Connectivity Challenges

by Howard Li

Technology Challenges

PC-based peripherals are being rapidly adopted by the embedded world causing low power technology to become increasingly critical. In handheld consumer electronics, Wi-Fi, LAN and Hard Disk Drives (HDDs) are being integrated into systems such as Smartphones, PMPs, and GPS systems.

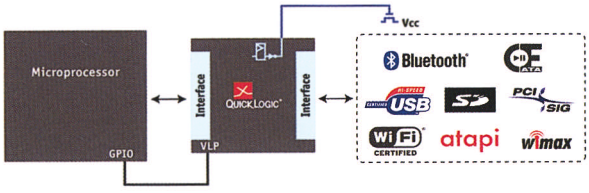
This trend has created two new major issues: interface connectivity challenges and the ability to minimize power consumption. With this in mind, QuickLogic® has developed seamless, power-efficient companion devices that connect from host processors, such as the Marvell®/Intel® PXA2xx and Monahans, to a variety of connectivity peripherals.

Featured Solutions

QuickLogic Companion Devices are complete connectivity solutions, which have been proven on the Marvell/Intel PXA and Monahans Platform Family, and include IP, software drivers and evaluation boards.

- CE-ATA-Based Hard Disk Drive via an integrated CE-ATA controller
- HDD or DVD ROM via an integrated IDE controller
- SD Card/SDIO, Wi-Fi, or Mobile TV via an integrated SDIO controller
- 10/100/1000 Ethernet, Wi-Fi or USB 2.0 via an integrated PCI controller

System Architecture



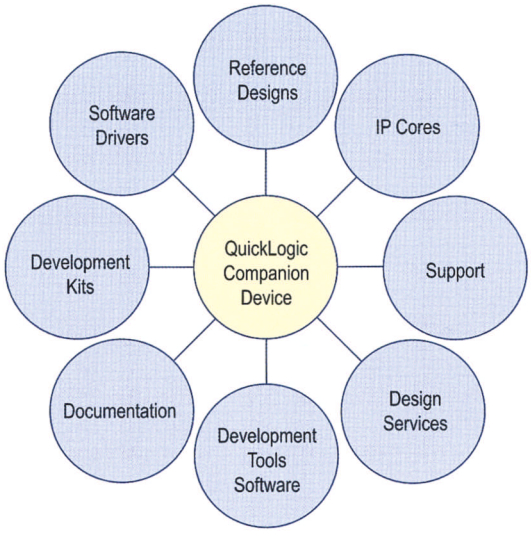
The QuickLogic Advantage

QuickLogic Companion Devices are a low power, small form factor, cost-effective solution that allows designers to reuse existing hardware/software and decrease time-to-market. These pre-programmed turnkey solutions work right out of the box allowing customers to simply drop them into their system and accelerate their design cycle. Further customization is possible with QuickLogic's programmable FPGA technology, enabling the customer to meet specific design needs.

QuickLogic Companion Device Solution

QuickLogic offers a complete solution pack to meet designer's needs as shown in the following illustration.

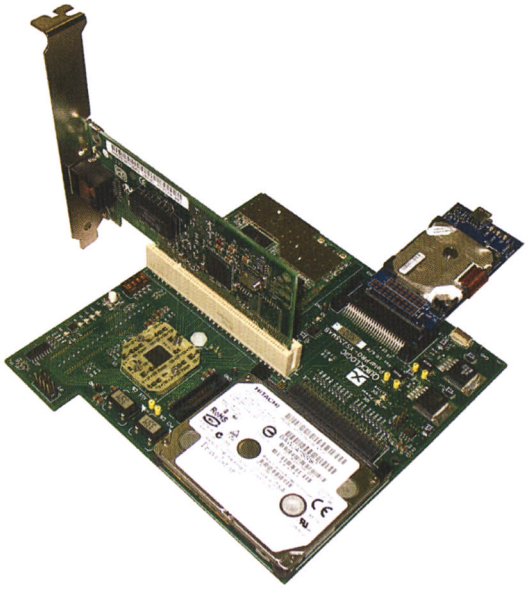
Solution Pack



QuickLogic Mobile Applications Board

The QuickLogic Mobile Applications Board is a daughter card that integrates with the Marvell/Intel PXA2xx Processor Developer's Kit to provide a platform for adding Wi-Fi, USB 2.0, Mobile TV, DVD ROM, HDD, CE-ATA hard drive, SD Card, and 10/100/1000 Ethernet connectivity to the processor.

Mobile Applications Board



Power Sensitive Applications

The growing convergence within the portable electronics market has resulted in low power becoming a supreme concern. Traditionally, ASICs have been used to resolve power issues, because the power consumption of FPGAs is too high a cost for their flexibility. Today with PolarPro™, QuickLogic's high density, low power FPGA family, designers can enjoy the benefits of flexibility and security without compromising their power budget.

The PolarPro Advantage

PolarPro FPGA technology was specifically architected to meet interconnect and system logic requirements of power-sensitive and portable applications. This family offers the lowest power programmable logic in the industry, drawing 2.2µA standby current. It exhibits ASIC-like power consumption in static, idle, and dynamic modes, extending battery life by 50x as compared to other programmable technologies. In addition, a small form factor Ball Grid Array (BGA) package is offered, which is critical for portable applications.

PolarPro Product Table

Device		QL1P075	QL1P100	QL1P200	QL1P300	QL1P600	QL1P1000
System Gates		75,000	100,000	200,000	300,000	600,000	1,000,000
Logic Cells		512	640	1,536	1,920	4,224	7,680
RAM Modules/FIFO		8	8	12	12	24	24
RAM Bits		36,864	36,864	55,296	55,296	221,184	221,184
CCMs		2	2	2	2	2	2
Packages (Max I/Os)	TFBGA (8x8)	132 (82)	132 (82)	132 (79)	132 (79)	—	—
	TFBGA (12x12)	196 (136)	196 (136)	—	—	—	—
	TQFP	144 (97)	144 (97)	—	—	—	—
	FBGA (1.0mm)	256 (172)	256 (184)	256 (184) 324 (238)	256 (184) 324 (238)	256 (184) 324 (238)	256 (184) 324 (238)

VLP Mode

A key feature of PolarPro's low power success is the proprietary VLP mode, which reduces power draw to 4 microwatts, while retaining I/O states, register values, and memory values. This enables longer battery life in applications that spend time in standby mode, making PolarPro the right programmable logic choice for power critical applications.

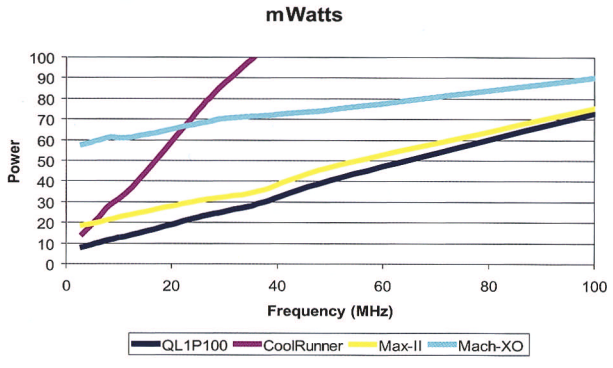
Dynamic Clock Disable

The two newest devices in the PolarPro family, the QL1P200 and QL1P300, have an innovative dynamic clock disable feature that allows designers to directly disconnect the clock trees in the PolarPro device on the fly. As a result, engineers can efficiently implement clock management schemes and lower the dynamic power consumption significantly.

Low Power Demo Board

To help illustrate the different programmable logic technologies currently available, QuickLogic has developed a power demo board. Each device has identical implemented logic function and operational frequencies, and is powered by an identical capacitor. The platform measures the number of times each device can execute the logic function before the capacitor discharge. As you can see in the following graph, PolarPro clearly outlasts the competition, exhibiting ASIC-like power consumption.

Low Power Demo Board Power Curves



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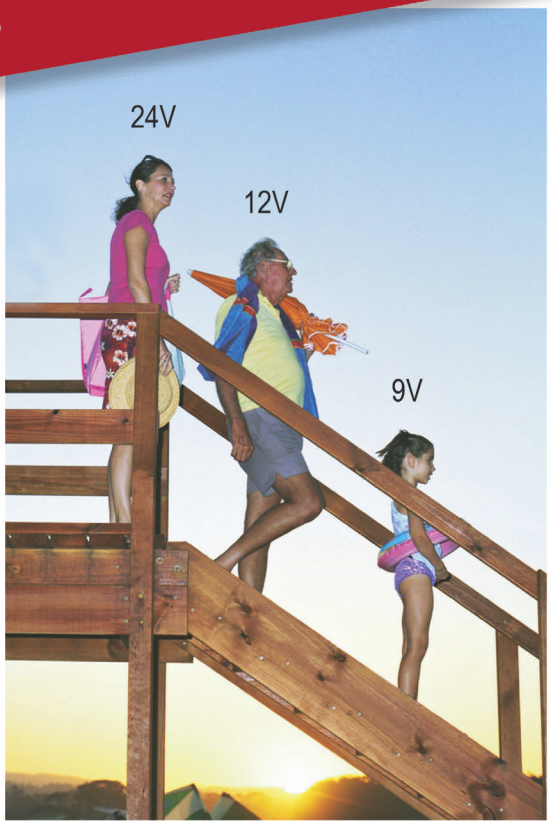

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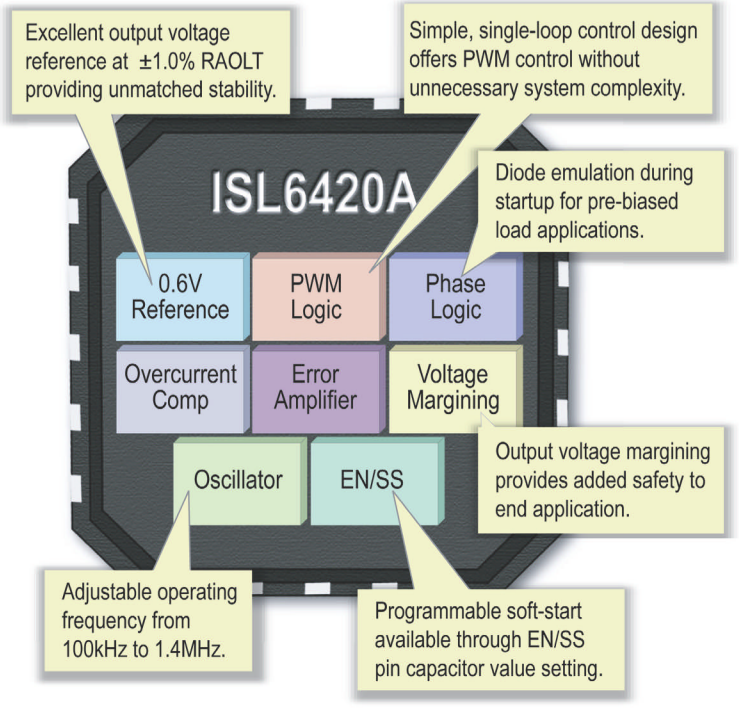
The ability to address a wide input voltage range of 4.5V to 28V gives the ISL6420A unmatched flexibility for use in most general purpose applications. It also has resistor-selectable switching frequency from 100kHz to 1.4MHz. Add all this up and Intersil has made choosing the right switching regulator for your design...well, like a day at the beach.



Key Features:

- Operates from 4.5V to 28V input
- Excellent output voltage regulation with 0.6V internal reference with ±1.0% RAOLT
- Resistor-selectable switching frequency from 100kHz to 1.4MHz
- Voltage Margining and External Reference Tracking
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Where does the energy go?

DANIEL VASCONCELLOS

In the early 1970s, I worked for Datapoint when it was the leader in distributed data processing. The company manufactured the first desktop computers, and the only reasonable method of program or data entry was a cassette-tape deck. Digital data is much more finicky than music; thus, the tape decks had constant-speed capstan drives, which were more rugged than an audio tape deck.

The capstan drive consisted of a brushless dc motor, four TO5 drive transistors, and commutation circuits. Datapoint put large numbers of computers with tape decks in the field, and the tape-deck-capstan motor drive had always been a source of field problems; the drive transistors failed sporadically. Because the drive problems came and went, the company lived with the problems.

Shortly after I was hired as an analog expert, the manufacturing team experienced many drive-transistor failures during endurance testing. I was directed to fix the tape-deck problems. The first step was to review the capstan-motor-drive history. The drive manufacturer had changed from TO5 transistors to TO92 transistors. After checking the maximum power-dissipation ratings, 500 mW for the TO5 and 350 mW for the TO92, I thought the solution was going to be easy. Replacing failed TO92 transistors with TO5 transistors reduced the failure rate from 60 to 1.5%. This reduction in failure rate is wonderful, but failing 1.5% of the time is garbage in my book.

So, I analyzed the problem. The transistor-power dissipation at the set power-supply voltage was 302 mW. I couldn't understand how a TO5 transistor could fail under those circumstances, so it was back to the lab and the factory floor to determine the real failure cause. The director of manufacturing was screaming because he couldn't ship computers with TO92 transistors. And I refused to change to TO5 transistors because their failure rate was unacceptable. The first day of lab testing revealed no conditions that could be responsible for a 1.5%-transistor-failure rate.

After more testing, I still couldn't find the failure mode. The engineering vice president entered the lab during elevated-temperature testing and questioned my sanity when he saw that the tape deck's ambient temperature was 100°C, the plastic was getting soft, and the tape deck was still running. But at least I knew that heat was not the problem.

The problem's cause had to be in the factory, so back I went. The endurance test was forcing failures, so I reviewed the test specifications: Nothing seemed wrong. I asked the manufacturing guys to help me set up the endurance test. During setup, I monitored tape-deck supply voltage because it was not supposed to change during the test. To my surprise, the tape deck's supply voltage increased 20%. A constant-speed motor is a constant-energy device; thus, the transistors dissipated the extra energy, causing their power dissipation to rise 453 mW in a 40°C environment. The endurance-test specification required the 5V power supply to be set to maximum, and, because the 12V supply was slaving off the 5V supply, the drive-supply voltage increased 20%. Now, it was easy to solve the problem by changing to TIP transistors with a 2W rating, and the transistors were in stock. The decreased failure rate more than offset the increased transistor cost. EDN

Ron Mancini is a retired engineer and a member of* EDN*'s Editorial Advisory Board.

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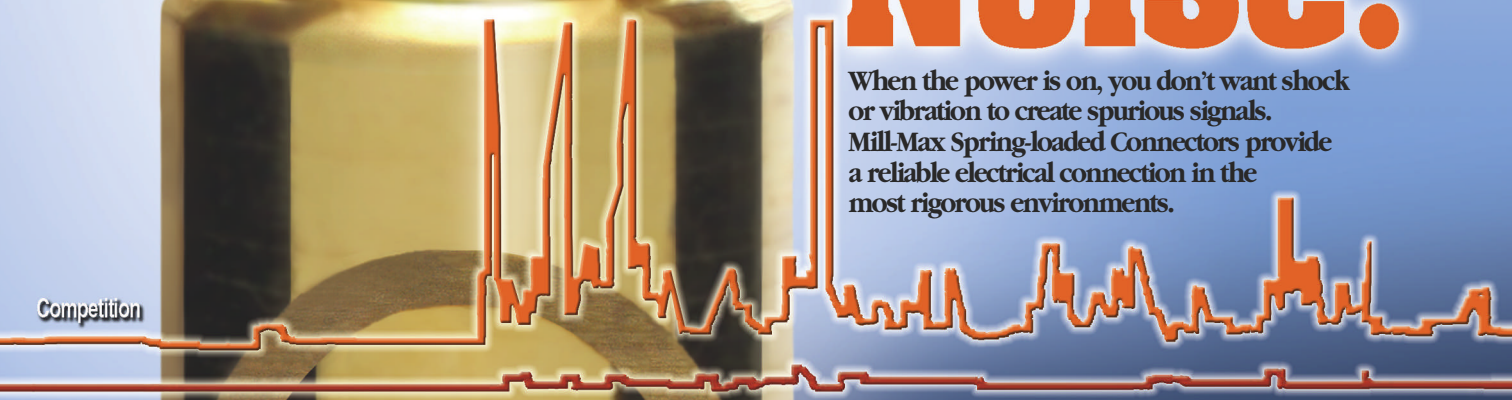

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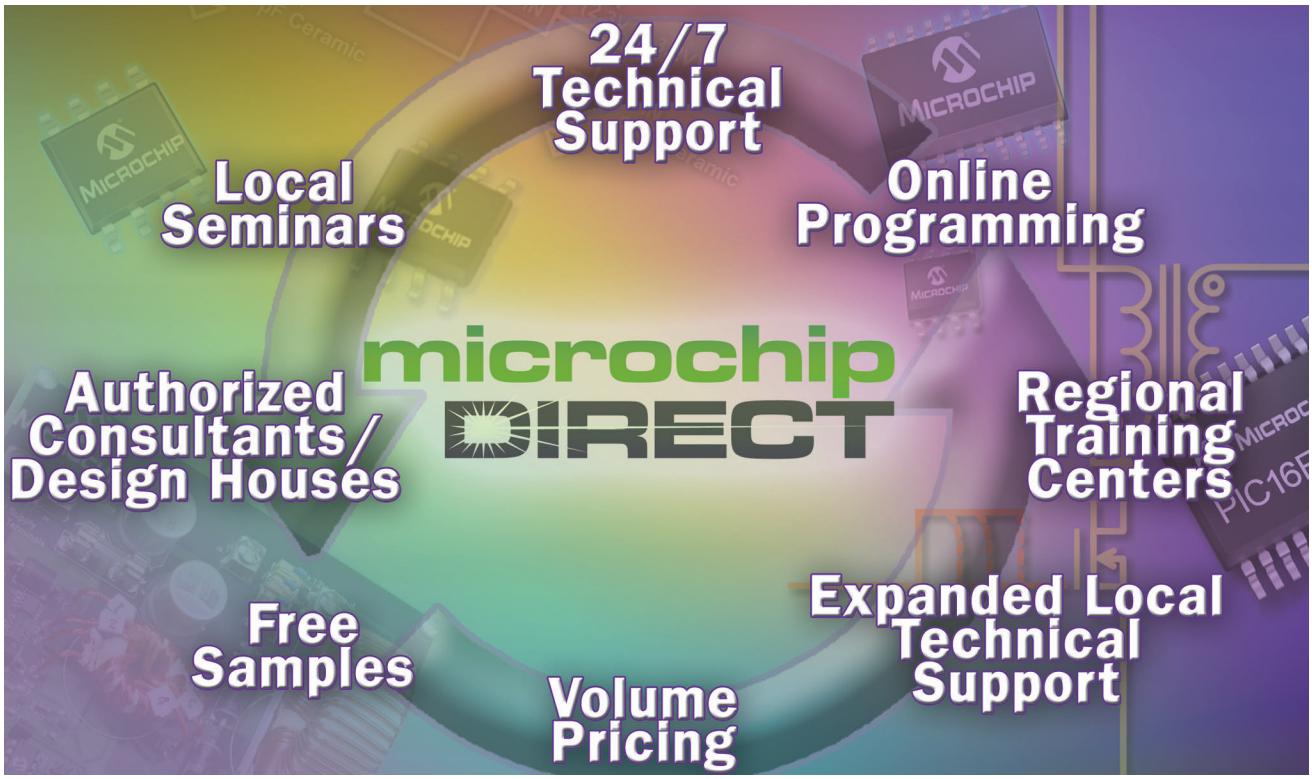

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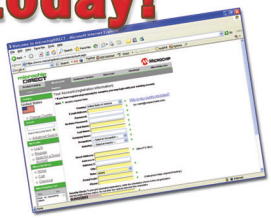

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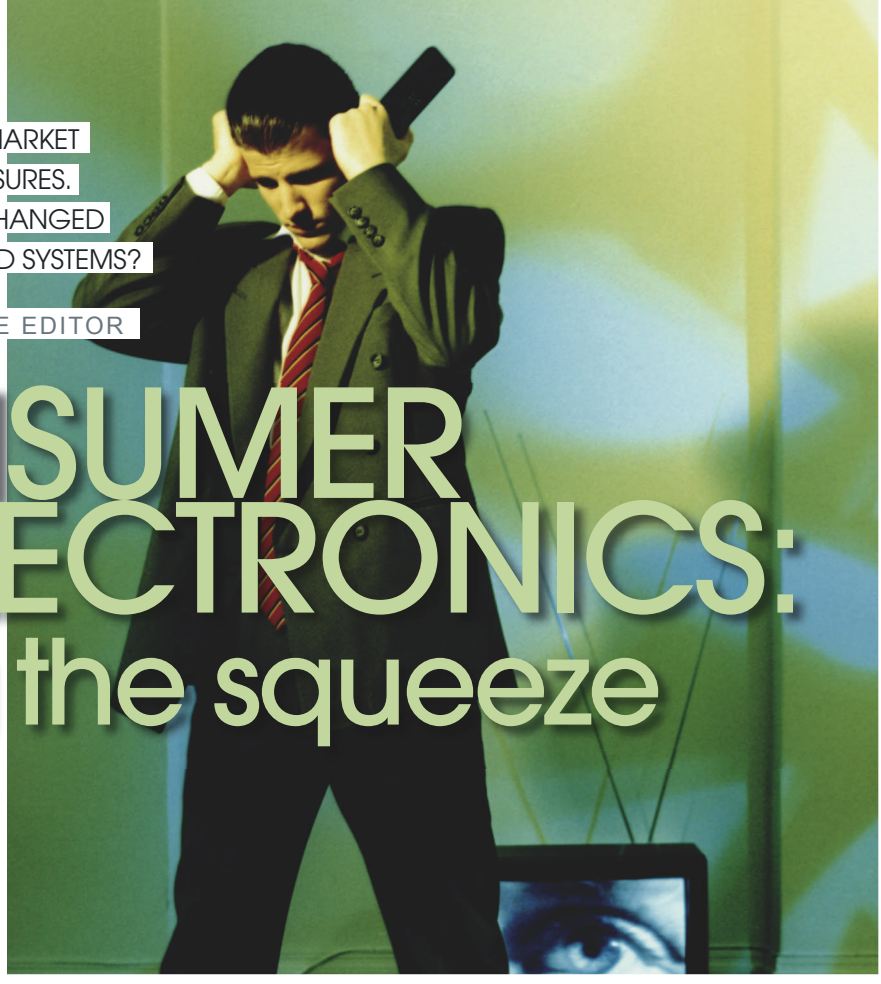
DESIGNERS IN THE CONSUMER MARKET WORK UNDER ENORMOUS PRESSURES. HAVE THESE CIRCUMSTANCES CHANGED THE WAY THEY DESIGN CHIPS AND SYSTEMS?

BY RON WILSON • EXECUTIVE EDITOR



CONSUMER ELECTRONICS: feeling the squeeze

The demands on consumer-electronics design teams are unquestionably different from those placed on other parts of the electronics industry: Have the new product on retailers' shelves by Thanksgiving, or kiss the company good-bye. Meet the cost targets, or we will cancel the design. Re-spin the silicon? No, just pull the plug on the project. And by the way, the final version of the video-compression "standard" we chose won't be ready—so, make sure you leave us enough processing head room to adapt to it with nothing but software updates.

The pressures on chip designers and system designers in the consumer world have been well-documented. All indications are that with global competition, low entry barriers to start-ups, and emerging local wireless and media standards, the pressures are just getting worse. What has not been widely discussed is how design teams are responding to these pressures. Are chip and system design soldiering forward in their traditional paths and just taking the risks? Or are we seeing a new style of design forming in the crucible of the consumer market?

Two of the forces crushing down upon consumer designers—schedule and cost—are familiar features of the arena. But today's fad-cycle consumer market has transformed them. There are two kinds of schedule pressure now, according to Arun Mittal, senior vice president and general manager of the power-management and -supply business unit of Infineon. "In some cases, the vendor is already present in the market, and [it is] enhancing [its] offering. In this case, total time to retail presence is the issue. In other cases, the customer is entering a new market area and must hit a particular window—usually the Christmas gift-buying season."

The dynamics of the two pressures are different. If the design is an enhancement or cost reduction, a schedule miss results in lost market share or reduced margins for a period of time. In the new-entry case—for instance, the original Microsoft Xbox—missing the Christmas window may mean having to wait another full generation for viable market share. In the one case, managers can make a rational trade-off between, say, a silicon respin and lost revenue. In the other case, missing is simply not an option.

Cost is also a more complex issue than it might appear. Often, consumer system designs will start out with a BOM (bill-of-materials) cost target, and the team will create the system around the hardware it can obtain for that price. "We see customers who start out by costing-out their BOM based on their anticipated volumes and then go from there," says Upendra Patel, chief technology officer of design-services company eInfochips.

"Consumer customers will often start with a fixed BOM cost and invest what-

ever is necessary in software-development time to make that hardware meet their system requirements," agrees John Dixon, DSP marketing manager at Texas Instruments. "Often, they are reliant on third-party design houses to actually do that work. So, in a way, the availability of design services becomes the real power of an architecture."

But cost is a more elusive figure than it might seem. At the very low costs typical of consumer electronics, complexity and cost become unlinked: A substantial change in the complexity of an SOC (system on chip) may have no major impact, but the resulting change in the cost of passive components or test time might be quite significant. The important thing, Infineon's Mittal emphasizes, is to look at assembled and tested system cost, not just BOM cost or—worse yet—chip cost. For example, he says, often the only readily available savings in a system are in the cost of the power supply.

Besides the traditional pressures, new issues are weighing down consumer-electronics teams. The most obvious of these pressures is power, which itself has two meanings. In ac-powered systems, less power consumption results in a less expensive power supply, less heat to expensively dissipate, and possibly greater long-term reliability. In a handheld system, the issue is not so much power—al-

AT A GLANCE

- Schedule, cost, and energy constraints have become huge factors in consumer-electronics design.
- Use of platforms and reference designs has grown rapidly.
- Many teams shift functions to software to respond to the pressures.
- Verification remains a major issue—even more important than in some other markets.
- The growing pressure could change EDA flows and fabless semiconductor companies in the consumer area.

USING A REFERENCE DESIGN TO SHORTEN PRODUCT-DEVELOPMENT-CYCLE TIME

By Gregory Eslinger, Acoustic Technologies

The growing demand for more complex products in less time increases the reliance of consumer-oriented design teams on highly integrated, high-quality reference designs. These reference designs can be ideal for wireless, multimedia, automotive, and telecommunication applications. Choosing the right reference design can increase the success of on-time delivery, lowering development cost and substantially reducing product-performance risk. More important, it can considerably reduce overall development-cycle time by as many as 40 weeks. However, finding a qualified reference design can be challenging, as the intensive process to fully develop a complete system requires a range of technical knowledge and skills from various third-party developers. When selecting the best reference design, it is important to consider the following areas:

- **Hardware platform: Does the hardware-design BOM (bill of materials) have the right price for your needs, the ability to quickly re-spin hardware for conformance to new plastics, and reasonable options for expandability?**
- **Platform support code: Does the platform have consistent, well-defined, and well-tested interfaces allowing third-party integration?**
- **System-function software: Does the system perform all required functions, including required third-party software? Does the ability to add additional software for future functions exist?**
- **Flexible user interface: Is the user interface flexible and simple enough to customize the human interface, allowing product differentiation?**
- **Robust testing mechanism: Does a testing mechanism exist, allowing for quick performance analysis of the final product?**

You can determine cycle time, cost, and risk reduction by addressing these five areas. As an example, consider Texas Instruments and Lyrtech's Bluetooth Hands Free Kit Reference Design, which is a compilation of expertise from third parties, including Acoustic Technologies and Adamya. This reference design has a stable hardware design and reduces cycle time, because it requires only one board spin. With system-support code already in place, designers can focus on adding value to their custom interface rather than spending months developing, debugging, and integrating what should be standard code. The Bluetooth stack and profile code alone can take months, if not years, to develop and test. Having a reference design that has already been integrated and tested allows designers to skip the time required for this necessary development and to focus on their user interface or other value-added features.

Once the product is complete, the ability to verify the final product performance immediately means faster time to production and ultimately allows the next-generation product to begin earlier. The right reference design that incorporates the hardware platform, system software, preintegrated and tested platform support code, and a flexible interface will significantly reduce risk, cost, and development time.

AUTHOR'S BIOGRAPHY
Gregory Eslinger is vice president of engineering at Acoustic Technologies Inc. He has more than 25 years of experience in embedded programming and managing embedded development for audio and video products.

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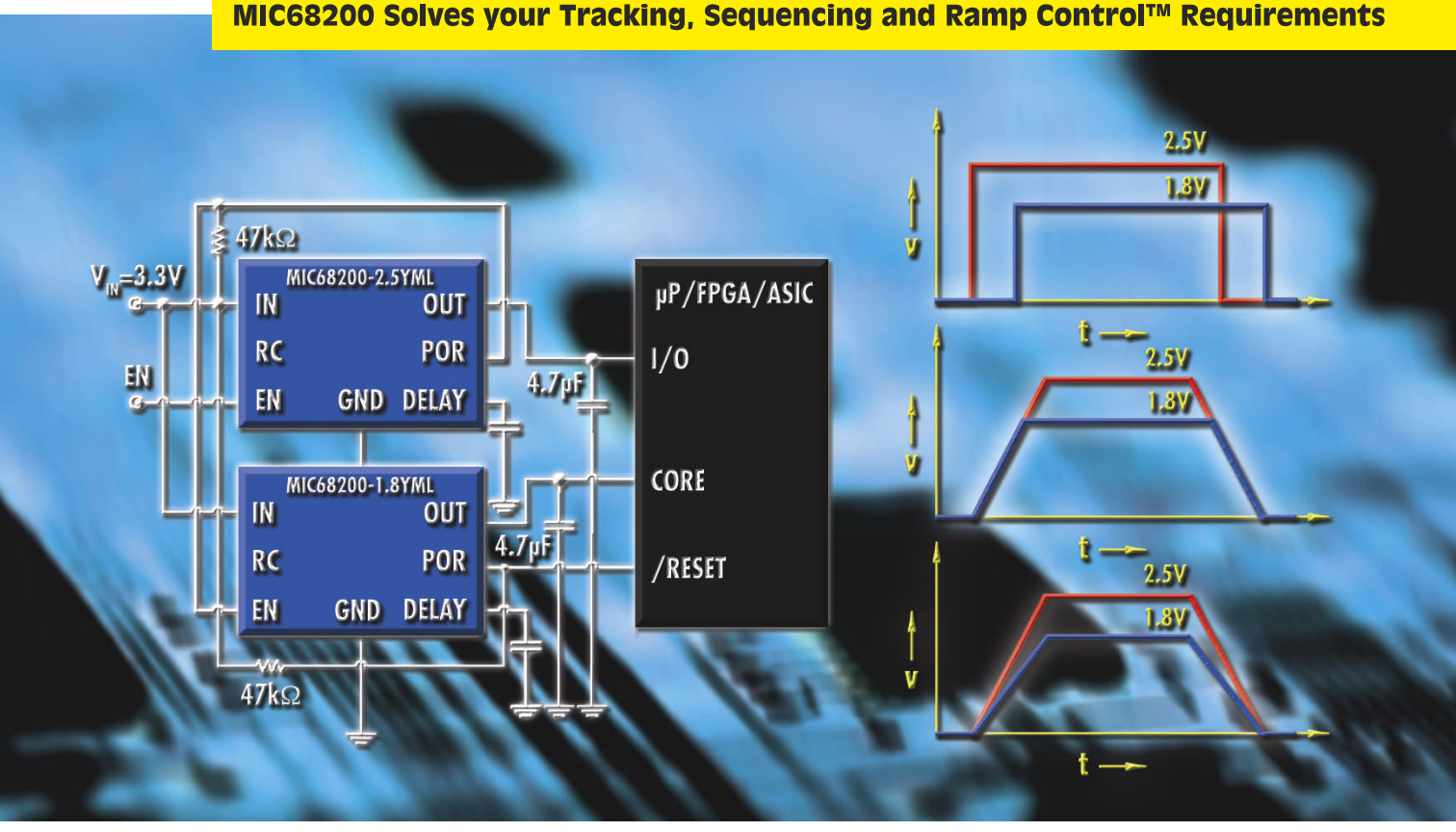

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though high-current-transient requirements can drive up the cost of a supply—as total energy per task, which is directly related to battery life. That metric is entirely different and can have very different architectural implications. For example, as Oleg Logvinov, chief executive officer of Arkados, points out, for net energy, it may make sense to move functions from efficient fixed hardware into power-inefficient software (**Figure 1**). Lacking the ability to completely power-down a block on the chip to halt leakage current, an infrequently used function may consume less total energy over a use profile if you do it on a less power-efficient CPU than if you do it on hardware that consumes less dynamic power but is quiescently leaking 99% of the time.

Another pressure that has been rapidly building on design teams is the number of technologies that a single system requires. Newport Media Chief Executive Officer and Director Mohy Abdelgany observes, "The complexity has grown so high that handset-chip designers are no longer circuit designers now; they

DRM LOOMS AS NIGHTMARE FOR DESIGNERS

As compact consumer devices pack in more and more functions, SOC (system-on-chip) designers are becoming used to the idea that they will be incorporating blocks into their chips that are quite unfamiliar to them. How, after all, is one design team supposed to be expert in cellular baseband processing, two kinds of CPU architectures, three memory architectures, four audio and two video codecs, video display, and 3-D-graphics processing?

But one design requirement on the near-term horizon looms like a gallows over chip designers and won't yield to any of the complexity-management schemes that have so far kept unfamiliar IP (intellectual-property) cores at bay: DRM (digital-rights management).

"We talk to customers who know they need a secure system to handle digital media. But they don't know what they mean by security," says Josh Kablotsky, vision fellow at Analog Devices (ADI). This situation necessitates a two-way conversation between platform vendors and system designers about the levels of security, their costs, and their practicality. ADI segment business manager Scot Robertson adds, "Customers start out wanting to protect data against every possible threat. Sometimes we have to explain the reality of the situation. This [area] is very unfamiliar for consumer-systems developers."

Security, according to Kablotsky, comprises two separate functions: ciphers and hashes to protect the data when it is outside the system and system-level measures to secure the operations upon the data, so that would-be copyists can't break into the system and divert the data in an unprotected state. The latter may include hardware to detect intrusion exploits, such as physically probing the chip, manipulating the power supplies, or intercepting the memory transactions.

The most powerful weapon systems designers have to protect themselves against unfamiliar technology is encapsulation–licensing the IP in such a way that they need to understand only the interfaces, not the function. But encapsulation depends upon the existence of standards, or at least commonly accepted definitions, for the function being performed. And that consensus does not yet exist for DRM. There's not even agreement on basic concepts, such as what ciphers are strong enough to work or whether, ultimately, hardware protection in the core of the system is necessary to prevent hacking.

And details within the DRM scheme can interact with system-level decisions to create vulnerabilities. "Chip architects have to understand this stuff in detail, even if they are following a reference design," Robertson warns.

Another attempt to work around this problem is to import a security scheme wholesale from a different market. ARM CPU director of product marketing Kevin McDermott said recently that he had seen customers licensing the company's SC100 Smart Card core for use beside a Cortex processor in some cellular-handset applications. The SC100 would provide hardware-secured authentication to protect other functions in the handset.

The second line of defense for many design teams is to learn about the technology by working intimately with a partner, and then taking over the effort. But so far, only a few design shops claim specialized knowledge of DRM. And, in any case, this strategy may never work. DRM is not a static fix to a static problem but–like intrusion detection or spam filtering–an ongoing war of measures and countermeasures, requiring full-time warriors. "There's a growing consensus that both Windows Media DRM-10 and Fairplay have already been cracked and will have to change," Robertson states. Nor is there any likelihood that a new DRM scheme will fare better. So once DRM enters the system, it will continually evolve. "This is a requirement for training, not for fixed solutions," Robertson says.

Altogether, the DRM scenario is near worst-case for systems developers. It is an ill-defined requirement; content providers won't even state whether they accept your level of protection. DRM cannot simply be licensed and integrated, and it requires frequent updates, maybe including revision to basic algorithms. Yet many perceive software–the typical way of permitting field upgrades–as much more vulnerable than hardware, so even a software-based approach may have to rest on a secure hardware core of some sort. And, in the end, the liability for any content that appears on the Internet could rest with the systems developer. There's a little added pressure for you.

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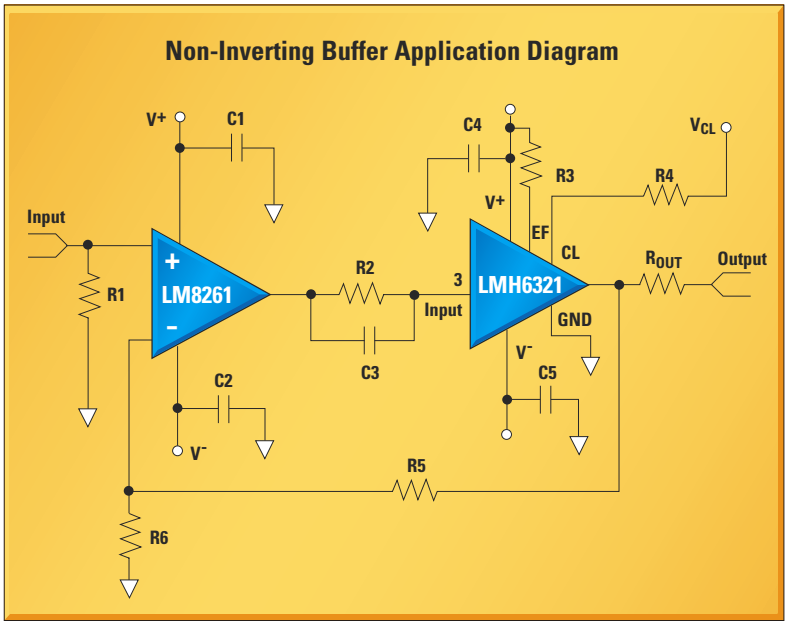

Product ID	Description	Features
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LMH6718	Dual, selectable gain buffer, Av = -1, +1, or +2	130 MHz SSBW, 200 mA Output current, 2.6 mA/ch supply current, 2nd/3rd HD: -84/-84 dB at 1 MHz
LMH6559/60	Single/quad, unity gain buffers	1.75 GHz / 680 MHz SSBW, 4580 / 3100 V/µs Slew rate, 74 mA output current, 3 to ±5V supply voltage range
LMH6739	Triple, 90 mA high-output current with shutdown	750 MHz SSBW, 3300 V/µs Slew rate, 11 mA/channel, 2nd/3rd HD: -80/-90 dB at 5 MHz
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are systems integrators. For instance, we are working now to put digital TV into handsets. The handset people don't know broadcast-television technology. They are dependent on their module vendors, and that is very uncomfortable for many of them."

Whether the module in question is for speech recognition, audio playback, 3-D graphics, digital TV, or GPS location, handset vendors are having to include functions whose details they don't understand. And handsets are just a leading indicator, not by any means an unusual situation in the consumer market. The trend is toward sweeping groups of functions you might desire in the same context—whether they are otherwise related or not—into a single package, and ultimately into a single SOC. Understandably, this situation stresses IP (intellectual-property) quality, reuse methodology, verification plans, and the nerves of design managers.

ARCHITECTURE RESPONDS

One of the primary ways consumer-electronics designers are responding to these pressures is with new architectural strategies (**Figure 2**). The simplest of these approaches involves letting someone else do the system integration—to license a complete reference design (see **sidebar** "Using a reference design to shorten product-development-cycle time). Although this technique is suspect to many US and European design teams, it is finding increasing favor in Asia.

Greg McNeil, product-marketing director for design kits at Cadence, relates, "Part of our strategy for having application-specific design kits is to include in the kit what we call a segment-representative design. It's basically a paper reference design that illustrates how the IP and tools would be used. When we show [it] to our North American customers, their response is often, 'Uh … Are you going to share that with the Asian companies?' The response of our Asian customers is more like, 'Great! Can I just start out with this [design]?'"

"We are hearing more and more about IP platforms," comments Terry Danzer, tactical marketing manager at ASIC vendor AMI Semiconductor. AMI has always seen customers willing to bring in IP that is necessary but not differentiating. But now, they are increasingly willing to bring in anything that is outside their specific area of expertise. And that may mean asking for a set of preintegrated IP that forms a complete platform under their specific hardware block.

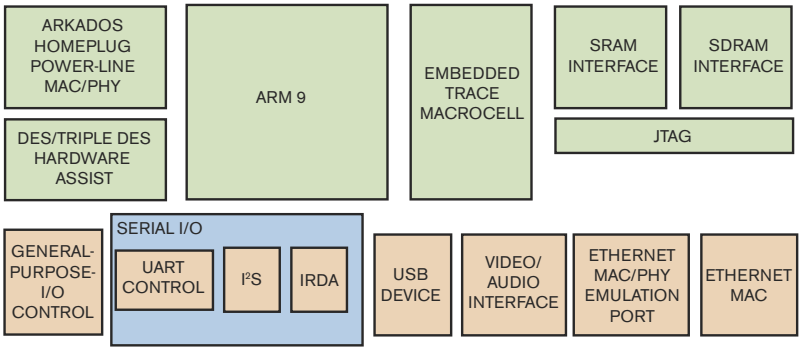

Figure 1 An early market entrant—in this case, the Arkados power-line-networking SOC—may choose to keep nearly all functions except interfaces safely in software.

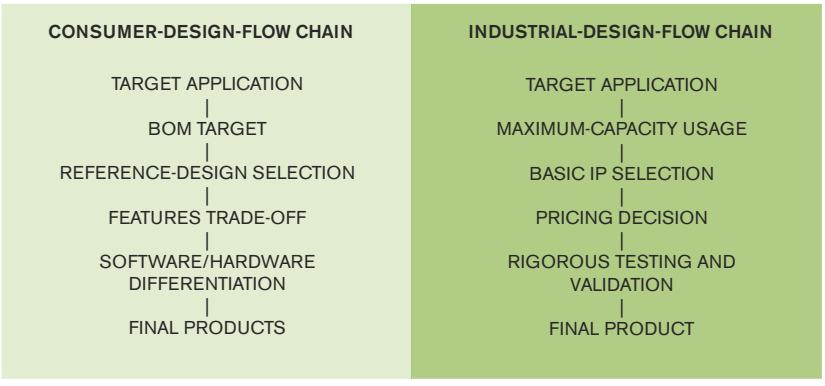

Figure 2 Design flows for consumer and industrial projects are diverging.

But a platform ASSP may be too large, expensive, and power-hungry for long-term viability in a consumer application. It's only virtue may be time to market. To counter this effect, many design teams are adopting a hybrid strategy.

"We are seeing what I'd call a kind of platform approach," says Newport's Abdelgany. "A company may start out with a relatively full-featured chip and do a series of quick spins to make minor modifications as [it learns] the specific needs of the market."

Vendors as large as Texas Instruments have used this strategy. For a recent customer entry into the portable-video-player market, for instance, TI scaled back its flagship Davinci SOC, editing the features, adding dynamic voltage scaling, and increasing the use of clock gating to produce a software-compatible device that consumes much less power. In this case, the effort was not small; it required a number of design teams around TI, all working to reduce the power of individual modules. But it was a much shorter effort than designing a whole new SOC.

In other cases, companies may simply remove blocks from their design, often coupling this effort with migration to a more advanced process to further improve die cost. "We are seeing a lot of derivative designs," says Cadence Vice President of Engineering Services Tim Henricks. "They are not trivial, but they are [much] cheaper than starting from scratch."

Henricks says that many customers initiate a chip design with a complete cost-reduction road map that will carry them through several generations of the chip, to the product's end of life. "This [approach] makes the availability of IP on future processes a real issue," he adds. "Especially with mixed-signal stuff, the IP vendors are reluctant to port their designs to a new process—like 65 nm today—until there's enough demand. So you have to be pretty big to be sure that

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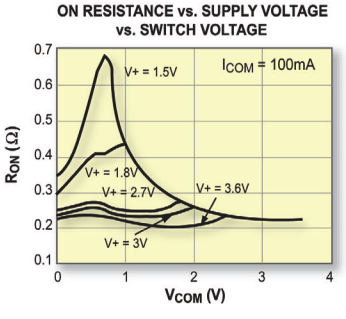
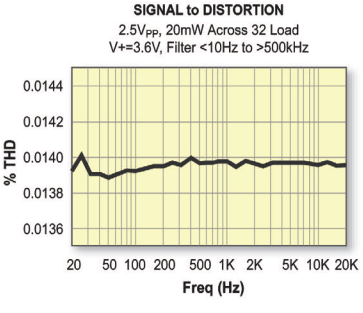
	Device	Function	R_{ON} @ 2.7V (Ω)	R_{ON} Flatness (Ω)	ESD (HBM)	Supply Voltages (V)	Packages
Singles	ISL84714	SPDT/2:1 Mux	0.44	0.06	6kV	1.6 to 3.6	SC70-6
	ISL84715	SPST (NO)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL84716	SPST (NC)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL43L210	SPDT/2:1 Mux	0.44	0.06	6kV	1.1 to 4.5	SC70-6
	ISL43L110	SPST (NO)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
	ISL43L111	SPST (NC)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
Duals	ISL84762	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL84684	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL8484	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 4.5	TDFN, MSOP
	ISL43L220	2xSPDT/2:1 Mux	0.23	0.03	9kV	1.1 to 4.5	TDFN
	ISL43L410	DPDT/Diff 2:1 Mux	0.29	0.03	9kV	1.1 to 4.5	TDFN, MSOP
	ISL43L120	SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L121	SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L122	SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L710	Diff SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L711	Diff SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L712	Diff SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
Quads	ISL83699	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 3.6	QFN, TSSOP
	ISL84780	Dual DPDT/Diff 2:1 Mux	0.45	0.07	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL8499	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 4.5	QFN, TSSOP
	ISL43L420	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.1 to 4.5	QFN
Octals	ISL84781	8:1 Mux	0.41	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL84782	Diff 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL43L840	Dual 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	QFN, TSSOP
	ISL43L841	Diff: 4:1 Mux	0.5	0.056	4kV	1.6 to 4.5	TQFN, TSSOP

ISL84684 Typical Performance





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SHIFTING TO SOFTWARE

Another key part of a platform strategy is to isolate blocks that are subject to change—either to serve multiple products with a single design, or to reduce risk from uncertain design requirements. This strategy requires encapsulating the block in a standard interface so that internal changes cannot impact the rest of the design. You can perform this technique by simply keeping the block in question in a separate chip, by carefully planning an SOC so that you can synthesize the new RTL into a particular block without major disruption, or by moving the function to programmable hardware or to software.

Conventional wisdom says that if you may have to change something in the future, you put it in software, or at least in an FPGA. And, in fact, the people we talked with for this article said that they often see consumer designs that implement functions in software—even when that approach is less than optimal from a power or performance standpoint—just to ensure time to market and the ability to go back and fix things later. "We see a lot more designs using more programmability, so that they can make adjustments after tape-out," says Paul Russert, Cadence's engineering-services group director. That measure may be absolutely necessary, because the verification effort for some blocks may extend past tape-out, as well.

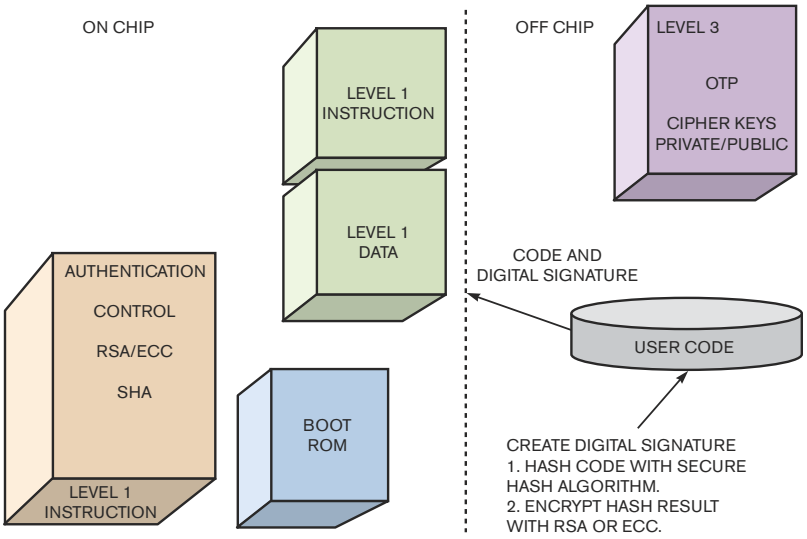

Figure 3 Functions such as digital-rights management may require complex blends of software and secure hardware.

As to how you should implement the programmability, violent differences of opinion exist. Some architects just keep things in software if at all possible (**Figure 3**). The appearance of instruction accelerators, DSP blocks, and more complex instructions on embedded CPU cores has greatly advanced that option. Some architects opt for dedicated but still programmable hardware. Tony King-Smith, vice president of marketing at IP vendor Imagination Technologies, says that in critical situations, Imagination's designers use scalable pipeline building blocks to create datapaths. The blocks are themselves configurable, so the resulting pipeline is programmable at the microcode level. Imagination then exposes this flexibility to its customers as various levels of abstraction, from driver code all the way to microcode. The result is a programmable element with great throughput and good energy efficiency, with several flexibility-versus-programming-ease points.

Newport Media's Abdelgany takes a different approach. "Our philosophy has been to enter a market with the lowest power and die size," he says. "For flexibility, we rely on the ability of our design teams to incrementally redesign the chip. It's not an easy game to play. You still end up with a fair amount of programmability, but where the customer needs it, not where it's convenient for the chip developer."

TABLE 1 OVERALL DESIGN CHAINS FOR CONSUMER AND INDUSTRIAL MARKET

Parameter	Consumer market	Industrial market
Volume	Very large	Medium
Customer's cost sensitivity	Very high	Low
Form-factor pressure	Very high	High
Royalty	Major deciding factor in price	Not a major issue
Maximum design efforts	Feature addition	Validation and hardware/software-standard compliance
Feature trade-off	Possible through phase- or model-wise approach	Not possible
Risk-taking ability of customer	Very high	Very low
Subsequent design changes	Very high	Low
Head room available for further customization	Large	Small
Selection of hardware components	Address current needs, work with recently introduced chips	Long-term availability and stability of the device in market
Time-to-market pressure	Very high	Low to medium
Design-team mindset	Time-to-market- and BOM-oriented	Compliance-oriented
Key differentiator	Supports software features and interfaces	Robust design and stringent standards compliance

CONCURRENT DESIGN

No matter what the architectural choices, unless a design team chooses to use an unmodified reference design, there will have to be an implementation cycle. Here also, consumer design is responding to pressure, mainly by employing various strategies for concurrent design.

The most obvious—and probably most frequent—strategies in this area are to make the hardware and software efforts concurrent and to modularize the hardware design, so that designers can

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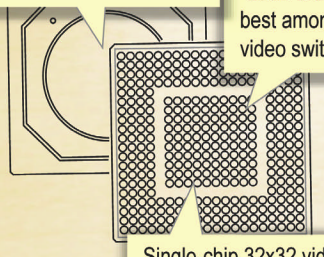
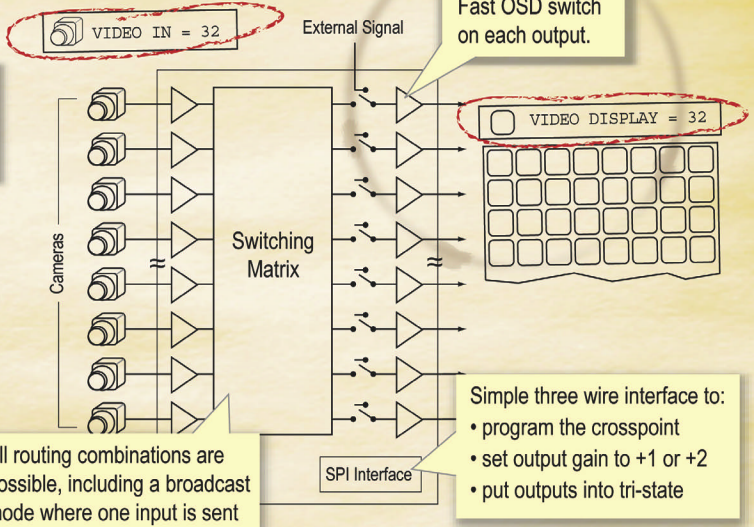


Single-chip 32x32 video crosspoint solution in 356 BGA package.



All routing combinations are possible, including a broadcast mode where one input is sent to all outputs simultaneously.

Simple three wire interface to:
- program the crosspoint
- set output gain to +1 or +2
- put outputs into tri-state

Analysis Results:
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- Buffered inputs and outputs
- Bandwidth of 320MHz
- Fast OSD switch for inserting text
- Crosstalk of -85dB at 6MHz
- Excellent video specs: 0.025%/0.05° dG/dP
- Broadcast mode provides 1:32 fan out
- Selectable output gain of 1 or 2
- Single, 356 BGA package

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concurrently design the modules. None of these ideas is even slightly novel, but design teams are applying them on a grand scale. And today, a grand scale often means implementation across global boundaries. A design-services team in California might design a chip for a shirt-pocket audio player using some IP blocks from the United Kingdom. This chip might drop into a board that a design team in India created, that runs application code that Romanians developed, on top of drivers that the Indian team wrote on a third-party kernel.

The key to this style of design is clear definition of the interfaces and specifications for each module. When you cannot encapsulate a module this way, the only viable alternative appears to be putting application engineers on site. In effect, management is matching the complexity of the interface between the blocks with the bandwidth of the interface between the design teams. It makes an intuitive sort of sense.

"You need reasonable project controls," explains Abdelgany. "But in the end, it may come down to our engineers working at the customer's facility. Sometimes we have won a design based on our ability to provide this level of application support."

In a time when everyone seems concerned about design outsourcing, this kind of recent experience has made Abdelgany bullish on the United States. "We are very fortunate to have a diverse work force," he says. "Our engineering staff includes people of Chinese, Korean, and European heritage. Almost anywhere in the world we can put an applications team on site and have someone who can serve as technical translator. But we have found that engineering is nearly an international language in its own right. Often the translation is needed mainly for interface to the marketing department."

VERIFICATION

Many consumer-electronics designers point to verification as the most serious issue that they face. On one hand, verification often consumes the largest share of development time. Design managers cite numbers greater than two-thirds the development time. So verification is an obvious place to respond to schedule pressure. On the other hand, in many consumer designs, a re-spin would be catastrophic. So verification must be even more thorough than it need be in markets that can meet initial orders with an FPGA-based option or can simply delay introduction by a few months.

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The first response of consumer-electronics teams to this situation is planning. "We see two kinds of teams," offers Cadence's Henricks. "Those who come in with a verification plan, and those who are still verifying after tapeout." That planning involves strategies for each of the blocks that will go into the system as well as a postintegration verification strategy for the system. And, increasingly, it will rely on some sort of coverage metrics. "Knowing when you are done is the biggest issue in verification," says Cadence's McNeil. "You may be talking about verification occupying 75% or more of the total design time, so shaving off a little bit is a big deal."

But knowing when to stop is also an unsolved problem. Coverage metrics can help, but none is definitive. A rigorous reuse methodology can help if it allows the team to reuse testbenches for individual blocks or even to adapt a system-level testbench from a previous design.

Once again, concurrency can be a friend. Starting system-level verification at the behavioral level and working down as block-level RTL and netlist verification work up can eliminate much of the calendar time. It can also help if the really hard tests can focus on areas that are problematic or have poor coverage. In some cases, if the verification plan requires designers to use assertions properly, formal techniques can augment dynamic testing with huge savings. "This [method] has to be design-savvy," says Henricks. "You have to know where the critical portions of the design are." And that information in itself can be a problem when the bulk of the design is a platform you license from another source.

An additional problem that distinguishes consumer-product verification is that the ultimate outputs of the sys-


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tem are often visual or auditory. There isn't an absolutely correct output—only wrong outputs and outputs that lie somewhere along a long scale of relative quality. Subjective judgments, often by golden eyes or ears, may be critical inputs into the verification process, and, without a parallel FPGA-based verification effort, these judgments may come very late in the schedule.

Unfortunately, despite all the planning and all the tools, the design manager's nightmare is all too common. "We see a fair amount of engineering-change orders coming toward the end of the design and coming from the verification process," Henricks says. To counter this situation, often consumer-electronics designers move critical functions into software, planning to use multiple software releases to fix late bugs and then reduce costs by converting the stable software modules to hardware engines. But even this strategy depends upon an art: being able to predict early in a design which functions will be the most problematic and will require post-tapeout flexibility. That ability can come only with experience.

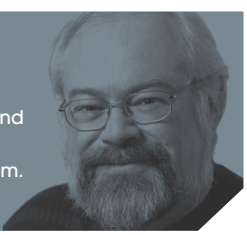
A PLATFORM FUTURE?

Clearly, there are many approaches to consumer-electronics design today. But all these trajectories may converge on a single trend line (**Table 1**). The use of platforms defines that line—whether hardware platforms in the shape of ASSP chips or IP platforms in the form of preintegrated blocks and flows. This way of thinking about consumer products has already become so pervasive that most IP vendors and many CPU and DSP vendors talk in terms of ecosystems—surrounding their products with all the other IP, hardware, software, services, and training necessary to quickly reach the final product.

These ideas about design will necessarily impact the industry in a number of ways. First, the increasing criticalness of verification is likely to force IP vendors out of their reliance on simple testbenches and into assertion-based-verification techniques. Even standards bodies, used to producing their result as an unreadable and ambiguous 1000-page document, are facing pressure to provide executable specifications in a property language.

Second, there will be growing pressure on EDA vendors to provide flows optimized not for completely new designs, but for the incremental design changes and platform tweaks that are the reality in the consumer world. There is no reason for a design team to allow all the degrees of freedom of a complete synthesis, place, and route cycle just to modify two blocks. Similarly, verification must become incremental. It must be possible for a static tool to prove the assertion that one modification has changed nothing else in the design.

Finally, the pressures of the consumer-electronics market may change the definition of a fabless semiconductor company. Suggests Imagination's King-Smith, "Increasingly, fabless companies are about marketing and about foundry relationships. The selection of IP, integration, and verification is increasingly taking place outside, in the ecosystems that are developing around particular applications areas." In this new future, the systems integrators may be the most powerful IP vendors, or the possessors of key proprietary knowledge about a new standard—a codec, say, or a digital-rights-management scheme (see **sidebar** "DRM looms as nightmare for designers"). Such a move would profoundly change the way the engineering-design chain works in this evolving market.**EDN**

You can reach Executive Editor Ron Wilson at 1-408-345-4427 and ronald.wilson@reedbusiness.com.


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EMBEDDED PLATFORMS: A SECOND LOOK

PROCESSING PLATFORMS AND THEIR SOFTWARE-DEVELOPMENT ECOSYSTEMS ARE BECOMING MORE IMPORTANT FOR THE SUCCESS OF DESIGNING INCREASINGLY COMPLEX APPLICATIONS.

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

During the last quarter of 2002, I did a hands-on project with Texas Instruments' OMAP (Open Mobile Application Processor) platform using the Innovator development kit. Although the article that resulted from that effort shared my experiences with the platform and the development ecosystem that TI had built around the platform, the article also touched on the issues of working with preproduction silicon and software; in essence, it was an early-adopter story (**Reference 1**).

Fast-forward to October 2005; TI announced its Davinci technology products and announced working product demonstrations within months of the rollout of the technology. The Davinci devices share a similar architecture with the OMAP devices in that they both integrate an ARM core with a TI DSP core in a single device. Doing a hands-on project with the new platform presented an opportunity to give a second try at developing on a similar complex-processing platform and to see how the development ecosystem that supports it had evolved over the past few years. Complex-processing platforms are not unique to TI, so, for the project, I also looked at platform offerings from other semiconductor companies to identify emerging trends for developing with these complex-processing platforms.

One thing that I learned from this exercise is that, although the silicon integration is a big part of the marketing focus for these platforms, the software assets and the tools that the platform provider provides are overshadowing or will overshadow the silicon to gain that much-sought-after design win. This statement is not an attempt to diminish the value and complexity of the hardware integration but an acknowledgment of the growing importance of the software assets and tools. This software simplifies the growing complexity of the software effort as a key differentiator between silicon offerings that provide increasingly similar integration and capabilities.

According to iSuppli (www.isuppli.com), by 2010, the total semiconductor market, excluding memory, analog, and

display drivers, will reach $163 billion from a bit more than $108 billion today, and about 88% of this market will be in processor-based offerings (**Reference 2**). All of those processor-based designs will need software. Gene Frantz, principal fellow and business-development manager for DSPs at TI, proposed in a recent blog entry that "the new twist on SOCs (systems on chips) is that the S is more likely to stand for "software" than "system."

According to Jay Gould, product-marketing manager for embedded processing at Xilinx, "The number of software engineers on a given project may outnumber the hardware engineers by a factor of two to five or more." Ata Khan, director of product innovation for the standard-IC-business line of NXP Semiconductors, and D Chris Baumann, director of BiCMOS products at Atmel, both point out: "For complex-processing applications, our customers' software development makes up 70 to 80% of their project's total schedule and budget resources." This percentage translates to a factor of 2.5 to four software-development resources for each hardware-development resource for these complex-processing applications.

The increasing focus on software is partly due to the fact that, with each advancement in processor technology, more software-instruction cycles are available to perform new value-added processing per sample period for a given application. For example, according to Frantz, in 1982, telecom systems could leverage 625 instruction cycles per sample period with a 5-MIPS processor. Today's modern DSPs can deliver hundreds of thousands of instruction cycles per sample period. He goes on to point out similar progressions, albeit with fewer instruction cycles per sample period, for audio and video applications.

The flexibility that software affords is a primary mechanism that these platforms offer to developers to add differentiating features and capabilities to their designs. Another contributor to the increasing resource allocation of software for embedded systems is based on an axiom I learned and adopted as an embedded-software and -system designer. For any problem, regardless of its root cause, if the software can detect the condition, can adjust for it, can minimize the effects of it, or even correct the condition, then, it is by definition a software problem. This axiom derives its truth from the fact that, in addition to being more efficient at performing complex serial operations than a pure-hardware implementation, software is almost always easier, faster, and cheaper to change than hardware, once the hardware exists.

The consequence of this axiom is that most faults that manifest themselves during the late stages of a design project directly flow into—and negatively impact—the software-development effort. This fact increases the complexity of the software far beyond just meeting the original product specifications, because the software must now accommodate unanticipated environmental and manufacturing variables without the need for changing the hardware if possible. The software-development team's success at accommodating the challenges of this axiom often represents the difference between successful and unsuccessful designs.

AT A GLANCE

- Complex-processing platforms are relying more on their development-support ecosystem for their adoption and success.
- Each iteration of platform offerings incorporates the lessons developers learned from previous iterations.
- Providing a development ecosystem is a huge effort, involving the growing pains of providing software assets for previously unsupported operating systems.

DAVINCI VERSUS OMAP

The Davinci and OMAP devices share some similarities. They both employ a heterogeneous-processing architecture that combines an ARM core with a TI's DSP core. They both support standard APIs (application-programming interfaces) that encapsulate and isolate the development and execution of the code residing on each core. For both device families, application programmers can use tools they are familiar with that target the ARM core; application programmers need not become DSP experts to take advantage of the integrated DSP core. Likewise, DSP

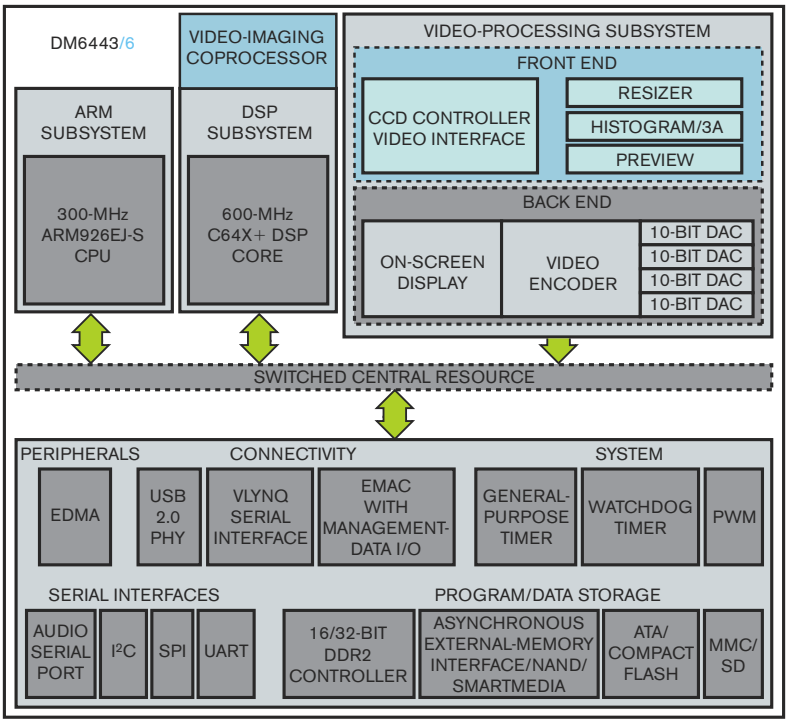
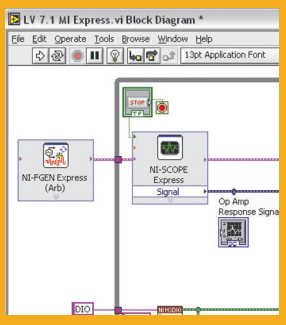
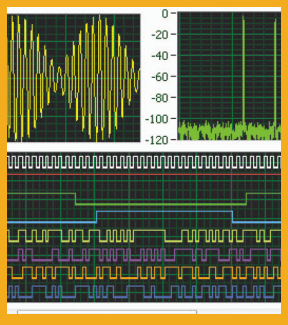
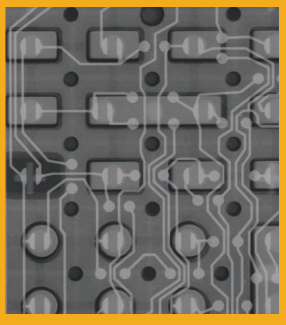
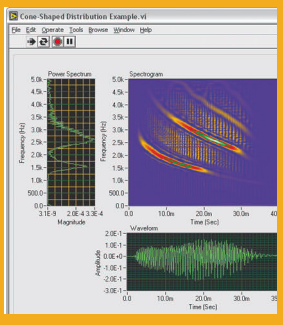


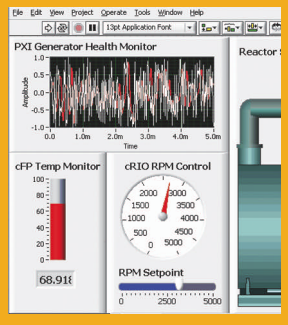
Figure 1 The Davinci devices have two processor cores and many storage, connectivity, and media-related peripherals.

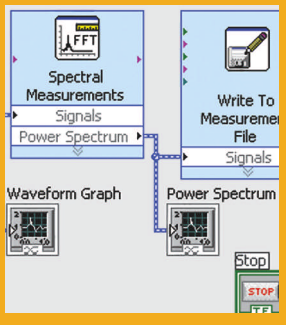





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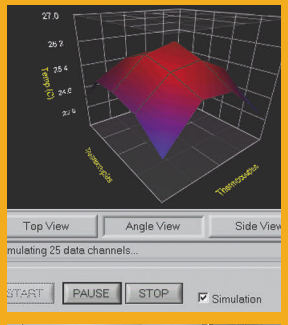



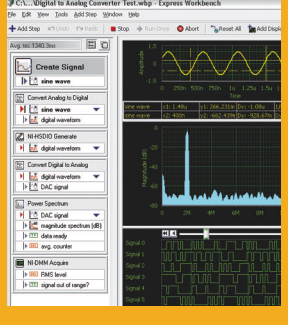

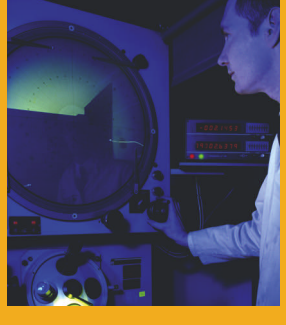
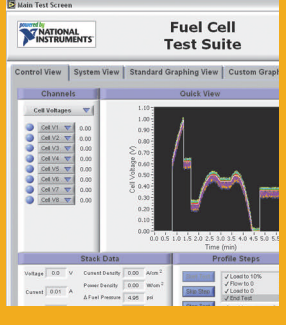

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programmers can use tools they are familiar with for the DSP core without learning about the ARM core. The Davinci and OMAP devices both use the eXpressDSP-compliant algorithms that are part of TI's third-party network, and they both support a primary execution model that places the ARM code in a master role and the DSP code in a coprocessor or slave role.

However, the Davinci technology differs from the OMAP platform in that Davinci targets digital-video and -audio applications rather than mobile applications, and it is an evolutionary step beyond OMAP with regard to software-development support. By virtue of their different target applications, the two platforms use different DSP cores. The OMAP employs power-efficient C55x DSP cores, whereas the Davinci employs high-performance C64x DSP cores. Also, OMAP devices use an ARM925 core, whereas the Davinci devices use an ARM926 core. Both sets of devices integrate different peripheral sets that are appropriate to their target-application domains. The integrated peripheral set in Davinci devices includes video-processing subsystems, serial and connectivity interfaces, and several memory and storage interfaces (**Figure 1**). The differences in the target-application domains drive these differences between the two platforms.

The Davinci platform builds on the lessons TI learned, both technically and businesswise, from the OMAP systems. For example, the Davinci platform extends the xDAIS (eXpressDSP Algorithm Interoperability Standard) with the xDM or xDAIS-xDM (xDAIS for digital media) interfaces. This interface affects each programmer's role—an application role for the ARM and a signal-processing role for the DSP—for a Davinci or an OMAP system; however, the interface is the mechanism that application programmers use to load, unload, and use the algorithms loaded on the DSP core. An important goal of xDM is to enable a plug-and-play architecture for multimedia codecs across various classes of algorithms and sources, or vendors. It defines common status and parameters for each class of multimedia codecs to facilitate replacing one codec with another without requiring a change to the application source code; only the configuration code for the codec needs to change.

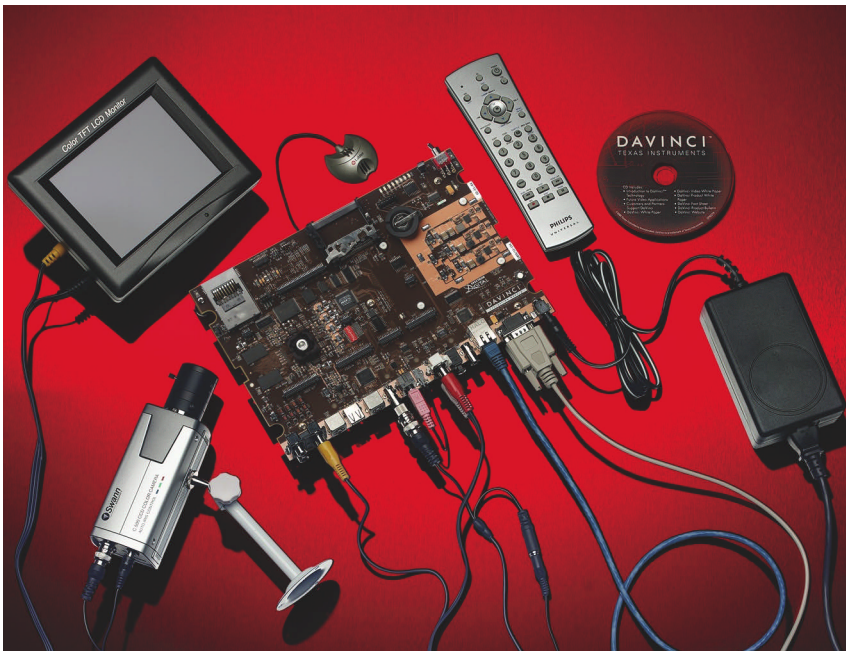

Figure 2 The Davinci evaluation module includes a camera, an LCD, an IR remote, speakers, and a hard-disk drive, as well as demonstration and development software.

The xDM standard defines and adds a uniform set of APIs for four codec classes—video, image, speech, and audio—to the xDAIS specification. The xDM's eight generic interfaces consist of an encoder and a decoder for each of the four codec classes. The xDM also supports extensions for requirements such as metadata parsing, file format, and custom processing. The xDM APIs add two new functions, process() and control(), to the xDAIS-defined set of functions. The call order of the interface-function calls is similar in the xDAIS and the xDM components except that xDM removes the algControl() method. When you use the xDAIS algorithms with xDM algorithms, the xDM control() method substitutes for the algControl() method.

Unlike the rollout of the OMAP, the rollout of the Davinci evaluation module includes three prewired DSP/codec combinations with which developers can work. The inclusion of the prewired codecs allows developers to evaluate the functions of the system without waiting for the implementation of production-supported codecs. The evaluation module comprises a kit that includes a camera, an LCD, an IR remote, speakers, and a hard-disk drive (**Figure 2**). The kit includes working demonstrations already stored on the hard drive to provide immediate access to exercising the encoding, decoding, and networking capabilities of the system.

Another difference between the rollout of the Davinci and the OMAP platforms was the immediate availability of chip- and board-level development resources for the ARM core. The Davinci evaluation module also included development tools and documentation to get started and work with the demonstrations. TI was able to include these components in part by limiting the development environment to Linux. Development tools for the DSP core are part of the Code Composer Studio tool suite. TI recently released two tools to support development with Davinci devices in late September 2006. The eXpressDSP configuration tool assists developers in integrating xDM codecs into the codec engine; formerly, the system integrator manually performed this process. The other new tool, the minimally invasive TMS320DM644x SOC visual analyzer, captures and displays data for both the ARM and the DSP cores on a single time line for a system view of the application behavior.

No amount of documentation can substitute for working directly with these complicated platforms: This proj-

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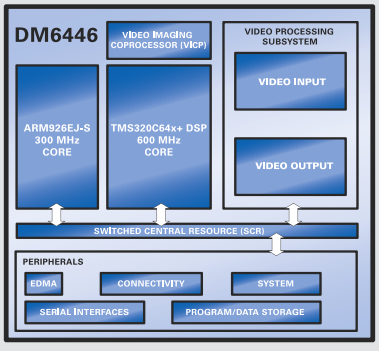
What is DaVinci?

Processors: Digital Video SoCs:

- TMS320DM6446 – Video encode/decode
- TMS320DM6443 – Video decode



Performance Benchmarks:

STANDALONE CODECS	DM6446	DM6443
MPEG-2 MP ML Decode	1080i+ (60 fields /30 frames)	720p+
MPEG-2 MP ML Encode	D1+	n/a
MPEG-4 SP Decode	720p+	720p+
MPEG-4 SP Encode	720p+	n/a
VC1/WMV 9 Decode	720p+	720p+
VC1/WMV 9 Encode	D1+	n/a
H.264 (Baseline) Decode	D1+	D1+
H.264 (Baseline) Encode	D1+	n/a
H.264 (Main Profile) Decode	D1+	D1+

+ denotes available processor headroom for analytics and/or other features

Tools: Validated Software and Hardware Development

- DVEVM (Digital Video Evaluation Module)
- MontaVista Development Tools
- Code Composer Studio IDE

Software: Open, Optimized and Production Tested

- Platform Support Package
- MontaVista Linux Support Package
- Industry-recognized APIs
- Multimedia frameworks
- Platform-optimized, multimedia codecs:
  - H.264
  - MPEG4
  - H.263
  - MPEG2
  - JPEG
  - AAC+
  - AAC
  - WMA9
  - MP3
  - G.711
  - G.728
  - G.723.1
  - G.729ab
  - WMV9/ VC1

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ect illustrated some disconnections between expectations and reality. Using a lesson I learned from the previous platform hands-on project, I went to a Davinci technical seminar. I thought the full-day session would be a hands-on workshop, but I was wrong. (The first hands-on technical workshop for Davinci would not occur until after I had finished this project and just before the print date of this article.) The technical seminar presented the technical and business aspects of the platform, but there was no hands-on portion. I was surprised by the number of Linux-implementation details the seminar presented. Later, when I had a Davinci evaluation module in my office to work with, I figured out why.

The first half of the seminar presented a nice overview of the system components and each of the peripherals, particularly some coding examples the video-processing subsystem uses. We learned about the Davinci Framework API and the high-level portions of each of the processing layers: application, signal processing, codec engine, and third-party software. The overview also covered the internal and third-party development tools that support each programming layer. The rest of the day consisted of third-party authorized-software-provider presentations.

I received a Davinci evaluation module to work with a few weeks later. It was a quick and easy process to connect all of the parts of the system and get the demonstrations operating correctly. My ability to get the demonstrations running quickly was due in no small part to the fact that all of the software resided on the hard drive. The nice thing, though, was that I could confirm that each component and interface was properly connected and operating correctly before setting up my workbench.

I received an unexpected shock when I went to set up my work space. I have done plenty of cross-platform development. For this project, I knew I would be developing to a Linux target. However, I didn't know that I would be working on a Linux-development host; I had assumed that I would be able to work on a Windows-development host. All of the initial tools for the evaluation module operate only on a Linux host. Montavista supplied the development tools, so I checked Montavista's Web site to confirm that it supported host environments besides Linux. The company's development tools support Linux-, Solaris-, and Windows-development hosts.

EMULATING LINUX WAS NOT A DEBILITATING EXPERIENCE, BUT THERE ARE DIFFERENCES IN ITS BEHAVIOR FROM WINDOWS APPLICATIONS.

TI's support personnel told me that the Davinci tools supported only a Linux-development host. I did not want to install Linux on my computer. This issue had nothing to do with a dislike of Linux; after all, Linux was to be the target operating system. Rather, it had everything to do with having to expend time, energy, and thought on a low-value effort for the project. I had no plans to continue using Linux on my host system, and I needed to fully understand the Linux configuration for the target. However, I lacked the time to relearn my host computer's operating system. Working in a Linux host environment increased my learning curve.

Fortunately, TI support shipped me a Red Hat Linux image and granted me use of a license for this project, so that I could emulate Linux on my computer with VMware player. This help allowed me to avoid manually setting up my computer for dual boot and to more quickly continue with the project.

I know how to find the data files and applications on my computer running Windows. The applications behave and interoperate as I have come to expect. I have years of lessons learned in how those applications behave. Emulating Linux was not a debilitating experience, but there are differences in its behavior from Windows applications. As an example, I used the supplied Gnome Ghostview to read the supplied Adobe Acrobat documents. I never could figure out whether I could perform a simple text-string search within the browser. I could have searched the Internet for a different browser, but why should I have to do that when I already have a perfectly acceptable browser?

The evaluation module supports only a Linux host because the Davinci-tools team wanted the tools to be available at the same time the evaluation module became available. Also, TI expected most of the early adopters to use a Linux target and would have experience with Linux as a development-host environment. The TI tool group acknowledged that support for other host-development operating systems is a next step. As it turns out, using Linux was also a significant learning curve for the TI support team because it had not worked with it before and because the team needed to be proficient with the system before the company started shipping the Davinci evaluation module to customers.

The project plan was to use the encoding-, decoding-, and networking-demonstration code to make a crude video phone. One problem was that I had only one Davinci evaluation module, so the demonstration could not perform in real time; I would have to simulate one end or the other of the system on each run. Obtaining the first evaluation module was a challenge; TI had only a limited supply. And there was not enough time to obtain a second module. Another problem was that the encoding and decoding examples that came with the module processed either speech or video data, but not both, so I had no example of how to synchronize the two. In my conversations with TI's tools group, I learned that the company was looking at the GStreamer media-processing library as a framework to help with audio and video synchronization and other capabilities. GStreamer sits above the level of a normal library. Late in the project, I started working with Ittiam using its video-phone demonstration.

For this project, I also tried out Green Hills Software's Probe and Multi development environment for Davinci. The Probe is a hardware-debugging device that connects to Davinci. Even though Green Hills Software's Multi normally supports development on Windows, Linux, Solaris, and HP-UX host systems, the Davinci tools operated only under Linux during this project. The Multi integrated development envi-

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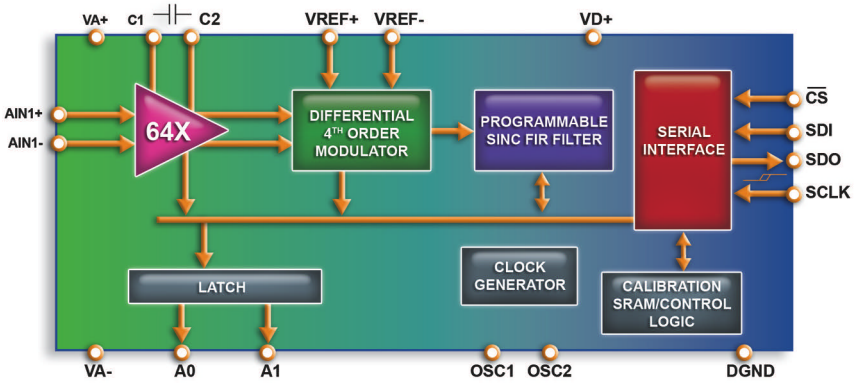

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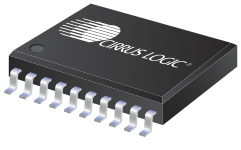
CS5532	24 bits	7–3840 SPS	±0.0015% FS	NMC	2	20 SSOP
CS5533	16 bits	7–3840 SPS	±0.0015% FS	NMC	4	24 SSOP
CS5534	24 bits	7–3840 SPS	±0.0015% FS	NMC	4	24 SSOP



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ronment supports the needs of each of the programming layers: application, DSP, and system. With the Probe, Multi provides visibility to both the ARM and the DSP cores, as well as supports Linux-kernel awareness. I was able to trace directly into the Linux kernel by building the Linux-kernel image with debugging information turned on and then translating, with Green Hills' dblink tool, the dwarf debugging information that GCC (GNU Compiler Collection) generated to a debugging format that Multi understands.

Multi separates process debugging into windows, each with its own background color; this feature is useful when using process-context breakpoints, which stops execution of the code only when the breakpointed line of code is executing as part of the specified process. I was also able to use the Time Machine capability; after you stop the processor core, it lets you step the instructions backward and forward. Green Hills recently added an always-on feature to Time Machine, which greatly increases its usability and helps developers because they no longer need to remember to turn on the Probe to capture an event.

BEYOND THE PLATFORM

Another difference between the ecosystems for the Davinci and OMAP platforms is that TI now offers to act as a first-tier point of contact for technical support and licensing of third-party hardware and software IP (intellectual property). This move simplifies the design team's efforts to acquire and use third-party IP and enables the support team to track problems and issues and more quickly share relevant information among those groups with similar issues. It also enables TI to more easily see trends in technical and business challenges, as well as requests for feature support, so that the company can react quickly to emerging opportunities.

The Davinci evaluation module includes another less obvious difference from the OMAP development kit that is consistent with a growing trend in embedded designs. Both platforms are heterogeneous, multicore systems. However, the Davinci module includes yet a third different processor core on the board to perform support functions: an ultralow-power, 16-bit MSP430 RISC mixed-signal microcontroller, which operates with and controls the nine LEDs, IR interface, and real-time clock on the system board.

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Employing multiple processing architectures is a growing trend for complex embedded-system applications. Examples include NXP's Nexperia platform, which combines MIPS cores with TriMedia cores, along with hardware accelerators and media-processing peripherals. The Nexperia platform employs an API analogous to the Davinci and OMAP platforms. NEC Electronics' EMMA (Enhanced Multimedia Architecture) platform features devices with as many as 16 processor cores, including 32-bit RISC, 32-bit RISC with DSP, and 64-bit RISC architectures, along with hardware accelerators and stream processors in the same device. An increasing number of tools simplify or help automate the creation and use of custom hardware accelerators and coprocessors for use alongside application processors and DSPs (**references 3** and **4**).

The continuing growth of complex embedded designs using multiple heterogeneous-processing architectures in a single design represents an area of opportunity for software-development tools to assist in system-level partitioning, identifying and implementing concurrency in software, and verifying operation and interoperability of all the processing engines. It also represents a glimpse at how the industry might be able to finally build and distribute reusable software components because developers could design each processing architecture or core to limit interaction with software on other cores. Platform providers can more safely provide commodity functions implemented as software on dedicated processors by locking access to those dedicated processors for all but those customers willing to risk breaking the encapsulation.

Mechanisms that support easier reuse and reliable interoperability of software components are critical capabilities for abstracting and scaling software complexity. To date, efforts to accomplish this goal have met with limited success, but domain-specific organizations are trying to specify and create a working model for interoperability between software components. Examples of such organizations are CE Linux Forum, the Digital Living Network Alliance, and the SDR Forum.

As the complexity of these processing platforms continues to increase, the support ecosystem for them will be more critical to the success of both the platform provider and partners and the design teams that use these platforms. A key concept that these early ecosystems are demonstrating is how a wide audience of application-level designers can rapidly and safely leverage and incorporate the work of a few expert users of a processing architecture in the context of a domain problem. EDN

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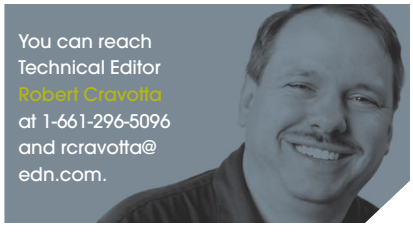

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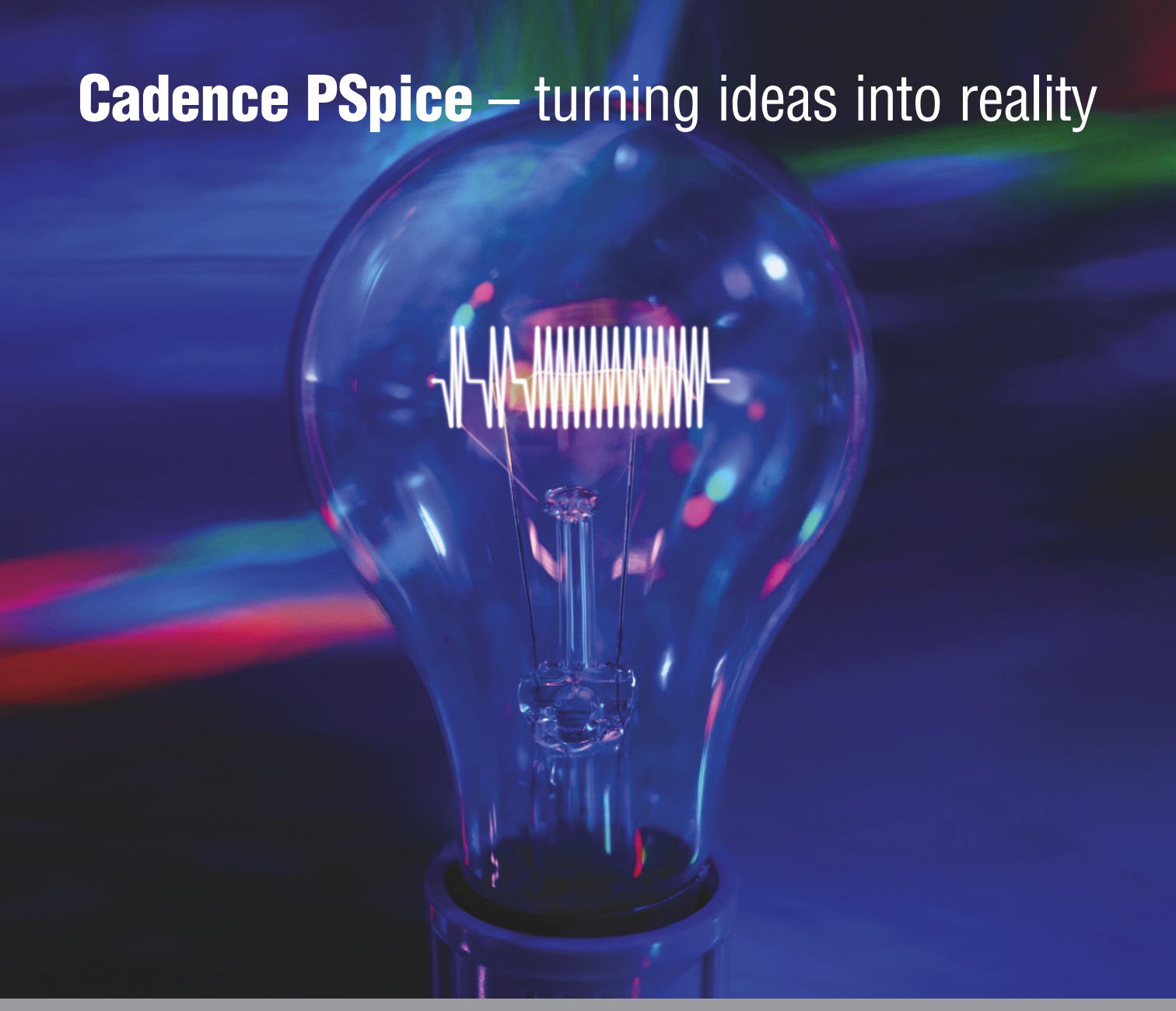

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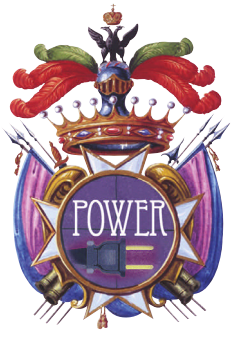
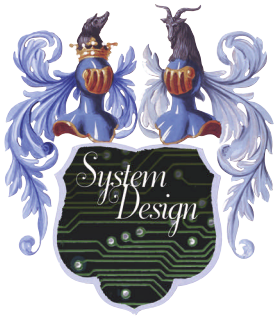
Global Report 3: worldwide analog, power, system, and IC design





In 2004, we conceived the *Global Report* as an annual project that would allow us to leverage our editorial resources worldwide and to address the global reader base with the results. Readers seemed to appreciate both the inaugural and the 2005 editions, so we now offer our third annual edition. Engineers worldwide face global issues, such as designing for international standards and regulations, and the potential of a global market for their work. We believe you will find that *Global Report 3* enlightens you in both regards. This year, our *Global Report* focuses on global issues centric to four design communities: analog design, power-system design, microprocessor-based design, and chip design. This *Global Report* includes a cornerstone article on each of the disciplines. Moreover, each of the sections includes sidebars to round out the coverage with information on other disciplines, products, and applications, such as test, programmable logic, and wireless communications.

In the analog section, Technical Editor Paul Rako addresses the fact that differing standards and regulations often affect the analog portion of a system design. In the power section, noted power expert Arnold Alderman, founder and president of Anagenesis, delves into the global concern over power-centric regulatory issues. This article provides a valuable resource and includes a sidebar on testing power systems. In the system-design section, Technical Editor Warren Webb offers an article that focuses on the choice of operating systems, including Linux, in hot applications. Moreover, our editors from around the globe have contributed additional insight into questions about which operating system will dominate in handsets, set-top boxes, and other applications. In the EDA section, our EDA expert, Senior Editor Mike Santarini, weighs in with an article covering IP (intellectual-property) issues in chip design. As you'll discover, you can obtain IP from many sources, and issues about securing IP and similar challenges remain as the global-design-engineering movement continues to escalate.

We'd also like to call your attention to the *Global Report 3* section of our Web site, www.edn.com/global. The Web portion of our report augments what you'll find in the print edition. For example, the Web offers a virtual global-round-table discussion involving our worldwide editors. Over the next few months, we'll also offer audio broadcasts and some global-centric newsletters for each section of *Global Report 3*. The newsletters will highlight additional Web material, including audio interviews with key industry executives.

Enjoy *Global Report 3*. If you find something you like or dislike, please e-mail me at mgwright@edn.com and let me know. Moreover, we encourage you to offer comments on the articles and sidebars in the Feedback Loop in the Web version of the material. EDN

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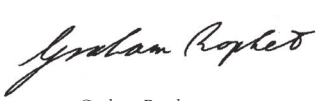

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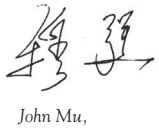

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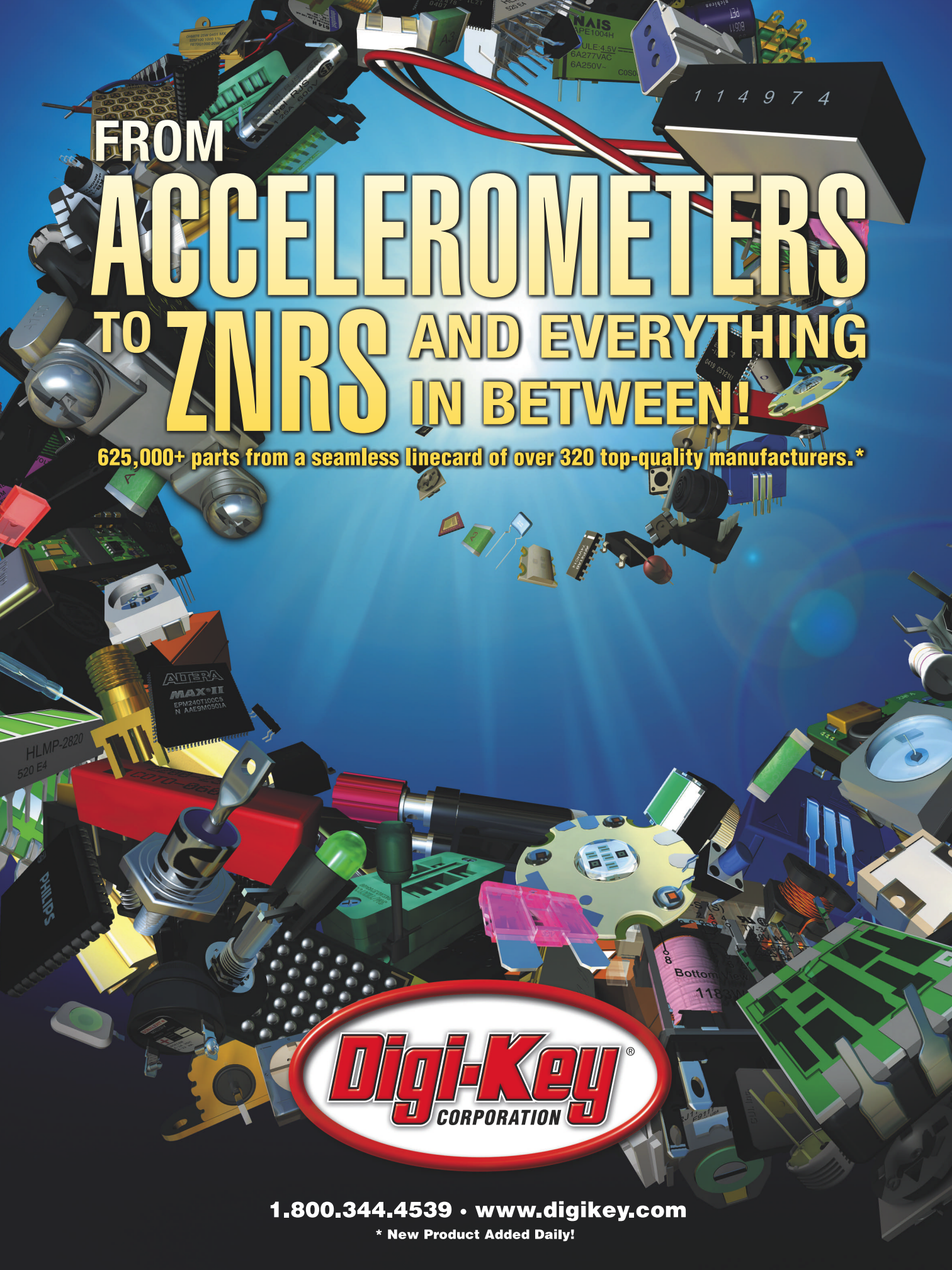
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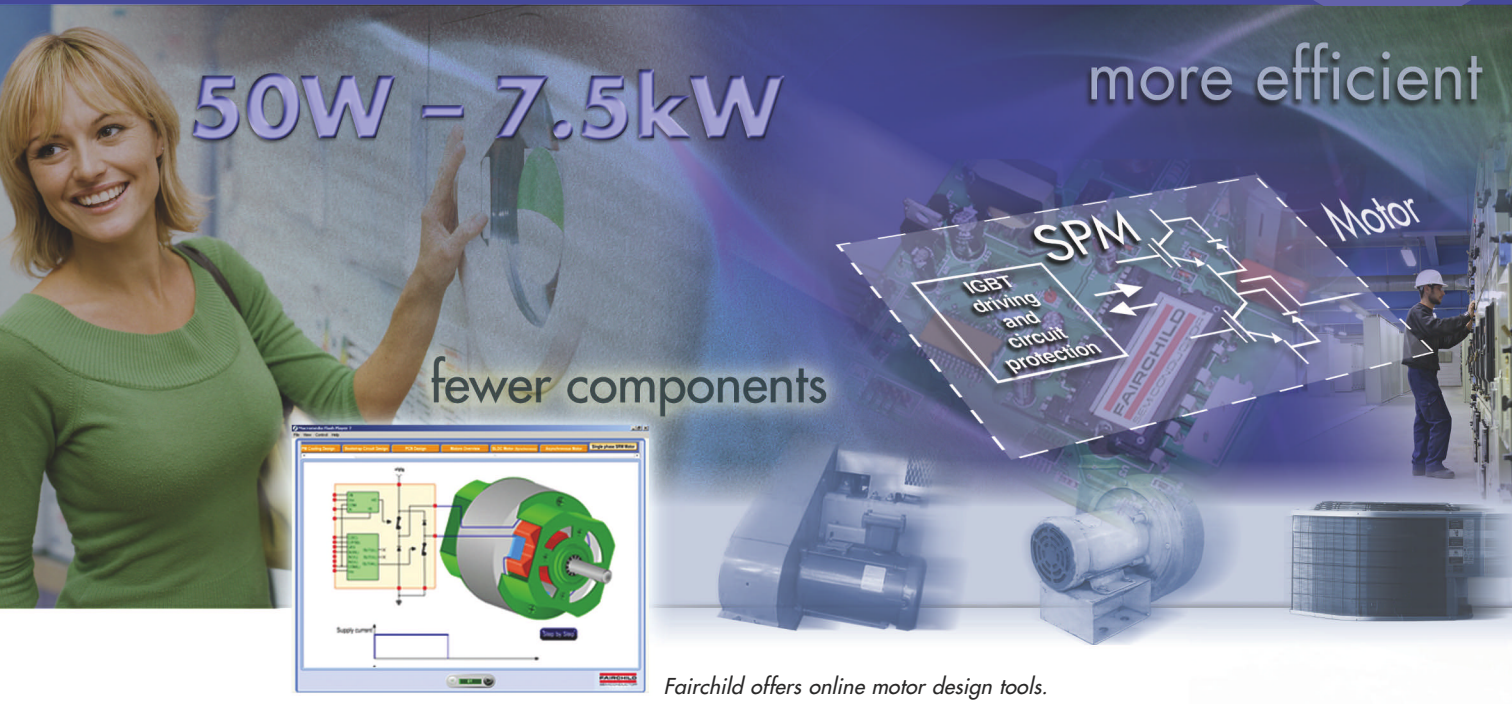

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GOVERNMENT AGENCIES ARE JOINING UTILITY COMPANIES TO REDUCE POWER CONSUMPTION BY TARGETING INEFFICIENT POWER SUPPLIES.

Surfing for market share?
Ride the efficiency wave

BY ARNOLD ALDERMAN, ANAGENESIS INC

Efficiency is a hot topic in today's power-supply market. Once relegated to a less important role, improved efficiency is now a major movement on a global front. There are two major reasons for this shift. First, power-grid managers have their backs against the wall today, with grids lacking capacity and global power consumption growing at an annual rate of approximately 2%. At the same time, the installation of more capacity has been meager at best, and not just in North America and Europe. Countries such as China, South Korea, and India are consuming much less power than the United States, yet they too face a shortage in power-grid capacity. Second, some high-tech installations, such as data centers, are reaching the point of meltdown. Heat generation has become a critical issue, prompting more than 70% of data-center managers to reveal in a recent poll that power consumption and heat generation are the most critical challenges they face. Currently, power supplies contribute 35% to those losses.

More efficient power supplies require better technology, which results in higher cost supplies. Improved technology is available now, but whether power-supply users are ready to pay more for their appliances or data-center equipment remains to be seen. However, mandatory state and country standards and efficient-equipment rebates are currently nurturing the acceptance of these more efficient power supplies.

"STANDBY"-POWER WASTE

In the late 1990s, people became aware that "off" did not necessarily mean off. TV manufacturers had for many years provided the "instant-on" feature, which meant that some circuits within the TV remained on, so that full warm-up would become unnecessary. The power required to keep these circuits on is known as "standby"-power consumption, and, according to a 2002 NRDC (National Resources Defense Council) study, it can reach more than 5W (**Table 1**). With millions of TVs throughout the United States consuming this power for most of the day, the study quickly calculated that standby power was wasting more than 158 billion kWhr of energy annually.

On Aug 2, 2001, President George W Bush issued an executive order establishing maximum power consumption at 1W (**Reference 1**). This order developed into a multifaceted set of initiatives, and the 1W standby limit became the norm for a number of consumer products. The "One Watt Initiative" has expanded globally, with participating countries creating the Standby Forum and officials assembling last November in Seoul, South Korea, for an international standby-power conference: Global Cooperation on One Watt (see **sidebar** "Energy programs around the globe"). The European Union Code of Conduct group has established its own standby-power-consumption standards (**Reference 2**).

TARGET: EXTERNAL POWER

With the success of the One Watt Initiative, agencies began to look for other low-hanging fruit. They realized that it was not the amount of power consumption per unit that was important but the *total* consumption. They immediately

identified the external power supplies as their next target (**Figure 1**).

The US EPA (Environmental Protection Agency) Energy Star program ranks potential ac/dc-power-supply power savings in its top-five list. According to Energy Star, increasing the efficiency of these supplies could save 32 billion kWhr of power per year—the same amount of energy that seven large power plants would produce—and potentially cut the US annual national energy bill by $2.5 billion (**Reference 3**). Most of the supplies that the CEC (California Energy Commission) and Energy Star evaluated consume less than 10W, but there are 2.5 billion of them in the United States alone. Test results from Ecos Consulting and EPRI (Electric Power Research Institute) Solutions in the United States and CECP (China Energy Conservation Project) in China reveal that many external power supplies provide less than 50% efficiency. Because external power supplies are supplementary items in low-priced consumer appliances, the market is highly cost-driven. Either incentives or mandatory regulations would have to nurture adoption.

TABLE 1 POWER-SUPPLY STANDBY-POWER MEASUREMENTS

Product	Manufacturer	Model	Standby power (W)
50-in. TV	Hitachi	50ES1k	3
27-in. TV	RCA	F27351wn	7
25-in. TV	Emerson	TC2556D	6
13-in. TV	Sharp	13J-M100	4
Stereo	JVC	RX-515VTN	2
Stereo	Pioneer	SX-201	2
21-in. monitor	Philips	PA1209	18
15-in. monitor	Applied Satellite Technology	7L	0
13-in. monitor	Impression	cm1448mk	0

Source: "Power supplies, a hidden opportunity for energy savings," an NRDC Report by Chris Caldwell and Travis Reeder, Ecos Consulting, May 22, 2002.

GENERATING A STANDARD

Typically, the standards-generation process begins with establishing the target product from energy

ENERGY PROGRAMS AROUND THE GLOBE

Many countries are implementing various programs to improve energy efficiency. For example, the United States has fostered better efficiency through the voluntary Energy Star program. Government procurement policies will impose the Energy Star standards on suppliers.

The EUCOC (European Union Code of Conduct) has established mandatory standby-power-consumption standards in cooperation with Energy Star, NRDC (National Resources Defense Council), and IEC (International Electrotechnical Commission). The EUCOC standard is the most aggressive standard established to date. The EU is now working on internal-power-supply standards. Even though Europe has constructed more new power plants than the United States in recent years, it continues to be aggressive with its efficiency and alternative-energy programs.

The CECP (China Energy Conservation Project) has a large energy-conservation-certification program. Both the CEC (California Energy Commission) and Energy Star used an extensive amount of CECP's test data to establish the power-supply-efficiency standards. CECP has a 3W standby-power standard for TVs.

South Korea's Energy Saving Office Equipment and Home Electronics Program is another voluntary-label program but with preferential government purchasing attached. It's a partnership between manufacturers and the Korean government's KEMCO (Korea Energy Management Corp).

Japan bases standards on the sales-weighted average efficiency of each manufacturer's shipment. The advantage of this approach is its flexibility. It leaves more freedom to manufacturers to adapt to the new regulation. They are free to keep energy-consuming equipment on the market, but they must stimulate purchase of more energy-efficient equipment to meet the sales-weighted average-efficiency target. The drawback of this approach is in the higher cost of the control process. Japan first introduced appliance energy-efficiency standards in 1979 as a reaction to the oil crisis under the Energy Conservation Law. Refrigerators and household air conditioners were the first appliances to meet the energy-performance standards. In 1984, the program discontinued standards for refrigerators, because all manufacturers had exceeded efficiency targets. In 1994, the standard incorporated guidelines for new appliances, including fluorescent lamps, televisions, heat pumps, copiers, and computers.

Australia is basically a "user" country, making its approach to efficiency standards interesting. Recently, the MCE (Ministerial Council on Energy) resolved to expand its commitment in reducing excessive standby usage. It will accomplish this feat by formulating a set of coordinated product-specific plans that will address excessive standby over the next 10 years, using the IEA (International Energy Agency) One Watt Initiative as a model. The country's new Top-Runner Program sets the standards according to the efficiency level of the most efficient product available in a given category. For each manufacturer, the weighted average efficiency of all units shipped within a category must meet the standards for that category.

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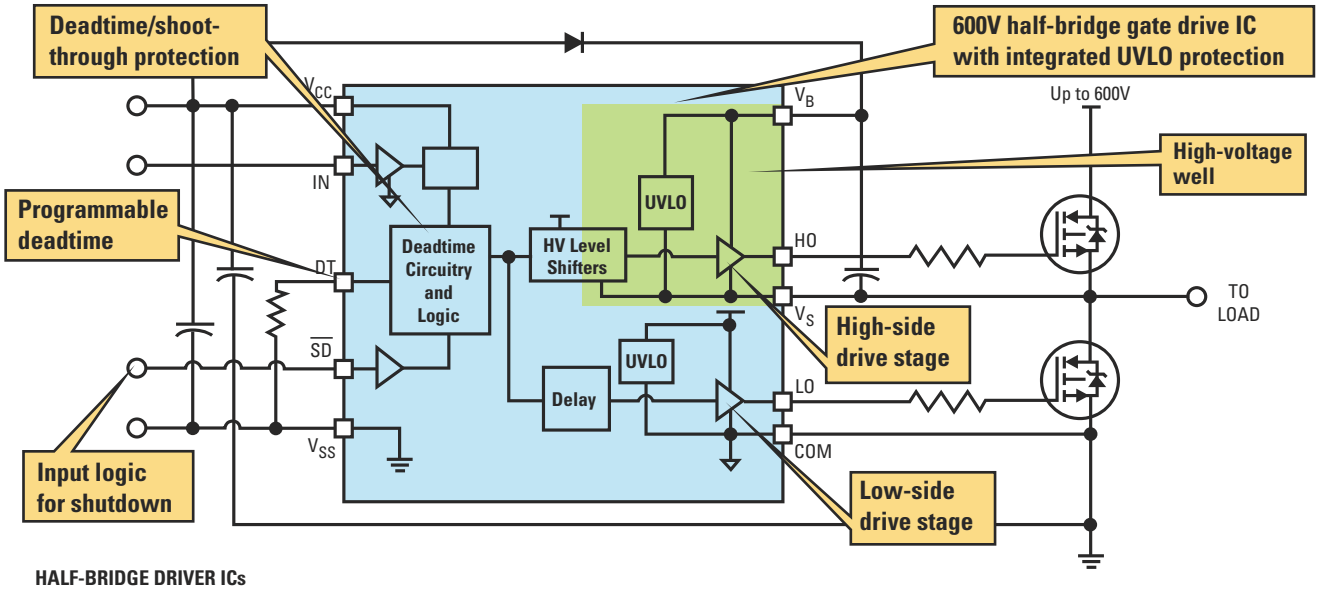

HALF-BRIDGE DRIVER ICs

Part Number	Pin Count	Sink/Source Current (mA)	Comments
IRS2103(S)PBF	8	290/600	UVLO V_{CC}
IRS2104(S)PBF	8	290/600	Input logic for shutdown; UVLO V_{CC}
IRS2108(S)PBF	8	290/600	UVLO V_{CC} & V_{BS}
IRS21084(S)PBF	14	290/600	Programmable deadtime; UVLO V_{CC} & V_{BS}
IRS2109(S)PBF	8	290/600	Input logic for shutdown; UVLO V_{CC} & V_{BS}
IRS21094(S)PBF	14	290/600	Input logic for shutdown; programmable deadtime; UVLO V_{CC} & V_{BS}
IRS2183(S)PBF	8	1900/2300	UVLO V_{CC} & V_{BS}
IRS21834(S)PBF	14	1900/2300	Programmable deadtime; UVLO V_{CC} & V_{BS}
IRS2184(S)PBF	8	1900/2300	Programmable deadtime; UVLO V_{CC} & V_{BS}
IRS21844(S)PBF	14	1900/2300	Input logic for shutdown; programmable deadtime; UVLO V_{CC} & V_{BS}

INDEPENDENT HIGH- AND LOW-SIDE DRIVER ICs

Part Number	Pin Count	Sink/Source Current (mA)	Comments
IRS2101(S)PBF	8	290/600	UVLO V_{CC}
IRS2106/IRS21064(S)PBF	8 / 14	290/600	UVLO V_{CC} & V_{BS}
IRS2181/IRS21814(S)PBF	8 / 14	1900/2300	UVLO V_{CC} & V_{BS}

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and environmental analyses. Next, you develop the test procedure and prove its accuracy, and all parties mutually agree on the results. Once you develop the standard and it receives approval, you test products to establish product-performance levels. You average that data and establish the first standard at some incrementally higher level. If the standard effectively alters the previous buying and producing patterns and saves significant energy, then it may undergo another iteration, increasing the performance level. **Figure 2** shows Energy Star's process.

In December 2004, the China MOF (Ministry of Finance) and NDRC (National Development and Reform Commission) jointly issued the procurement policy for energy-efficient products and first List of Energy Efficient Products for Government Procurement (known as the Energy Efficiency List). The policy requires that government organizations must give priority to the energy-efficient products that the list specifies. In 2005, the central, first-level budget units and provincial budget units implemented the procurement policy. In 2006, the implementation will extend to central, second-level budget units and first-level budget units in cities and regions. In 2007, it will achieve full implementation. **Table 2** lists state programs at work within the United States.

Figure 1 Following the success of the One Watt Initiative, the industry took aim at external power supplies (courtesy Ecos Consulting).

Until recently, vendors stated power-supply efficiency only at full load. However, as most people know, few supplies see full load at any point in their operating cycle. In the past, typical power-supply efficiency dropped off significantly at lighter loads. Intel Corp was one of the first to require minimum efficiency at other load points in its VRMs (voltage-regulator modules) and VRD (voltage-regulator-down)-supply specifications. The CEC and EPA have more recently adopted that approach, basing their overall power-supply-efficiency calculations on measurements at 25, 50, 75, and 100% load.

There are several modes to consider for internal power supplies, such as those in power supplies, TVs, TV set-top boxes, and workstations: standby, active, off, idle, and sleep. The governing document usually defines these modes. An internal power supply is more complex than an external power supply, due to its multiple outputs. Currently, there is significant debate about how to state the overall power-supply efficiency with so many outputs. For

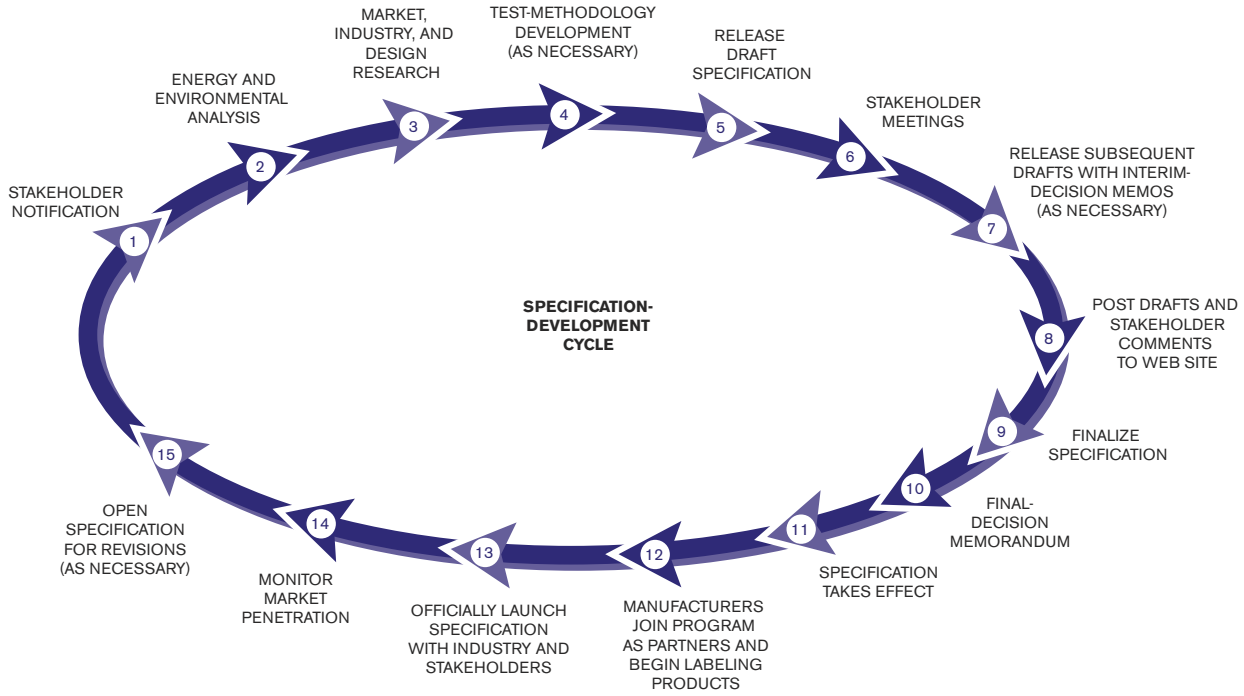

Figure 2 Energy Star's standards-generation process begins with establishing the target product from energy and environmental analyses.

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this reason, the internal-power-supply standards are taking longer to draft and adopt than those in the industry originally expected.

The 80 Plus Program is an incentive program that utility companies sponsor. The objective is to provide higher efficiency power supplies in PCs. These supplies must have better than 80% efficiency over the *entire* operating-load range of the power supply. To date, participating utilities have contributed more than $5 million of incentives (**Reference 4**). Current procurement policies will have to change for the 80 Plus Program requirements to become mainstream. Some optimistic advocates

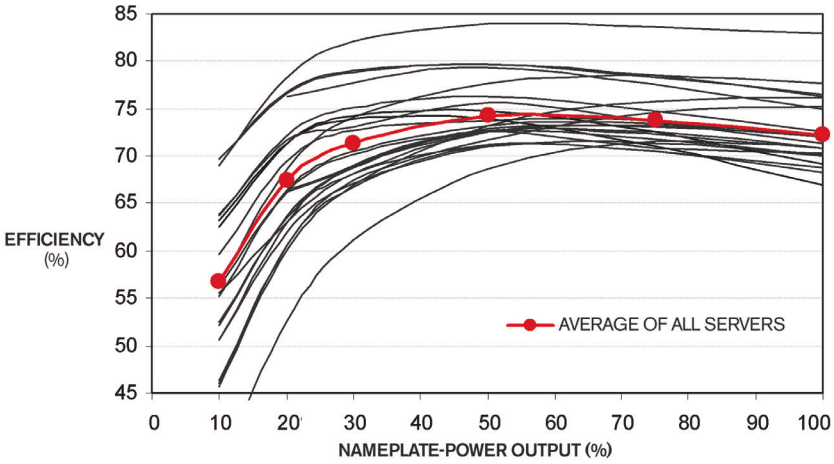

Figure 3 In a double-redundancy situation in which the power supply would operate at 25% power, the efficiency ranges from 58 to 82% (courtesy Ecos Consulting).

DSOs SPEED POWER-SUPPLY-DESIGN VALIDATION AND TESTING

By Dan Strassberg, Contributing Technical Editor

Improvements in power MOSFETs, regulators, and control circuits have made switching power supplies smaller and have enabled power densities greater than 1W/in.^{3} with efficiencies exceeding 90%. Product life cycles are shrinking rapidly, and competition is becoming tougher. When designs are similar, a shorter time to market or a shorter production cycle can make the winning difference. By using features unique to digital oscilloscopes, engineers can now considerably reduce power-supply-test time.

DSOs (digital-storage oscilloscopes) acquire waveforms as sequences of numbers, enabling the automation of many complex calculations. Among DSO attributes that are useful in power-supply testing are:

- **A DSO can capture single-shot phenomena, such as power on/off or failure conditions, synchronously on as many as four channels.**
- **Nearly all DSOs automatically calculate pulse parameters and perform basic waveform mathematics (calculate sum, difference, product, ratio). Most DSOs can also perform more complex mathematical operations, including integration, differentiation, calculation of exponential functions and logarithms, extended averaging, digital filtering, and determination of extreme values and FFTs (fast Fourier transforms).**
- **In addition to internal hard drives that can store reference waveforms, most DSOs allow external storage—now usually in the form of USB-compatible memory sticks. Users can thus save waveforms as graphics files and create high-quality hard copies.**
- **DSOs offer a wealth of trigger capabilities. They can trigger on fault conditions and enable users to view pretrigger data to understand the conditions that caused the fault.**
- **Most DSOs store instrument setups in nonvolatile memories. Users can easily recall these setups either manually or under computer control. Predefined setups can be part of fully automatic (or semiautomatic) test sequences, eliminating the need for time-consuming manual adjustments.**
- **DSOs commonly offer several types of automatic pass/fail testing. A user can define a mask waveform and specify that any input waveform must be contained within the mask. Alternatively, the user can select a set of waveform parameters, which the scope automatically calculates and compares against predetermined limits. If the waveform or the parameters fall outside the desired limits, the scope can take several actions, including freezing the display, saving or printing a copy of the aberrant waveform, sending an e-mail or instant message to the appropriate engineer, or producing an audible alarm. The DSO also tracks the statistics of passing and failing events.**

Figure A shows the power-on transitions in a multivoltage power supply. The simultaneous monitoring of all such transitions is useful for verifying that any phase shifts are within acceptable limits. In fact, any voltage imbalances could be damaging to the load circuits. You can also automatically calculate the switching time, as the figure shows.

THIS IS A HOLDUP

The holdup time is the time for which the output voltage remains stable, at full load, after the loss of ac power. A digital oscilloscope is the ideal instrument for measuring holdup time because of both the powerful trigger system and the single-shot-capture capability. (This task usually requires an oscilloscope

expect that a 90 Plus Program might be next. Industry suppliers claim that the technology is available.

HELPFUL TRENDS

Adding more copper and iron to the linear supplies or replacing the linear supply with a switching supply can create more efficient external power supplies. In the past, the incremental cost was significant. However, in the past four years, the price of copper has increased by 500%, significantly reducing the change in cost for more efficient power supplies (**Reference 5**).

Another major movement within the power-supply industry is the implementation of digital control. It potentially offers the hope that core digital control will mean better control for optimized efficiency for all operating conditions by possibly including full I/O-power monitoring, multiple-topology operation, power-optimization control, the need for fewer converters through the use of an alternative architectural structure, and the elimination of redundancy.

DATA-CENTER MELTDOWN

Data centers are heating up as facilities install more equipment to meet increasing information-processing requirements or the consolidation trend. Many multinational companies are moving from many dispersed centers to a few megacenters. Power density will double over the next five years (**Reference 6**). Industry participants now see power consumption and heat generation as critical. Planners are finding improved power-conversion efficiency attractive due to the double savings possible—less power loss and less cooling. The process does not lose power but conveys it to the load, and the reduced losses yield less heat, which reduces the cooling requirements and costs.

When you look at a double, or N+1, redundancy situation in which the power supplies are often the most stressed components, and it is important to verify that their operating points lie inside the safe operating area. The product of the drain-to-source voltage and source-current traces shows the power dissipated in the transistor. You can also completely automatically perform the safe-operating-area test. By selecting the peak-to-peak parameter and applying it to the dissipated-power trace, a user can specify a maximum peak-to-peak power. If the test fails, the scope can stop the acquisition, print out the failing waveform or store it in memory, and beep or otherwise notify the user. In another approach to automatic testing, the user simply takes an acquired waveform and specifies the desired tolerances. When the test activates, the scope verifies that all input waveforms fall inside the mask. In case of failure, the scope can take any of the previously mentioned actions.

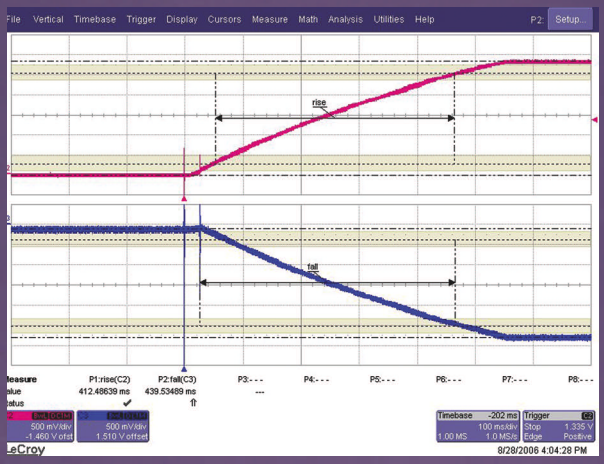

Figure A The switch-on transition of a dual-output (5 and −5V) power supply often requires that the two voltages display symmetric behavior. The automatic calculation of pulse parameters (rise and fall times, in this case) simplifies the test.

with deep memory.) Some manufacturers call the trigger condition "dropout trigger." The scope triggers when the pulse train on the ac line disappears for more than a specifed length of time.

At power-on, the input current that the power supply absorbs exhibits a spike that should not exceed the maximum allowable input current. The oscilloscope uses a dual-slope trigger. That is, the scope would trigger on Channel 1 for either slope of the input pulse, provided that the pulse amplitude exceeds 0.5V. The scope can automatically test the inrush current in two ways. It can calculate the peak current value and verify that it is smaller than a preset limit, or it can compare the full current waveform with a reference mask (as the European Telecommunication Standard pr ETS 300 132 requires). If the test fails–that is, if the inrush current exceeds the set limits–several actions are possible.

The oscilloscope can compute power by capturing the voltage and current waveforms at the power-supply input, deskewing any timing shift that results from different current/voltage-probe lengths. The oscilloscope must then multiply the waveforms point by point to provide the input-power waveform, from which the scope can automatically calculate a mean dc value. The ratio of the output power, also a dc value, to the mean input power is the power-supply efficiency.

A DSO can make single-shot measurements of a supply's high-frequency switching noise and can calculate the waveform's FFT. Frequency analysis of the output noise can give valuable information about the noise's origin.

In a switching power supply, the switching transistors are

AUTHOR'S BIOGRAPHY

Dan Strassberg holds a bachelor's degree in electrical engineering from Rensselaer Polytechnic Institute (Troy, NY) and a master's in electrical engineering from the Massachusetts Institute of Technology (Cambridge). He has been covering test and measurement for EDN since 1987.

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TABLE 2 STATE APPLIANCE AND EQUIPMENT ENERGY-EFFICIENCY STANDARDS

	AZ	CA	CT	MA	MD	NJ	NY	OR	RI	VT	WA	2005 federal energy law
Status	Enacted 2005	By regulation in 2002, 2004, and 2006	Enacted 2004	Enacted 11/05	Enacted 2004	Enacted 2005	Enacted 2005	Enacted 2005	Enacted 2005 and 2006	Enacted 5/06	Enacted 2005	NA
Automatic commercial ice makers	X 2008	X 2008					X 2010	X 2008	X 2010		X 2008	1/2010
Ceiling fans and ceiling-fan-light kits		X 2006			X 3/2007		X 2007					1/2007
Commercial clothes washers	X 2008	X 2005/2007	X 7/2007		X 3/2007	X 2007/2010		X 2009	X 2007		X 2007	1/2007
Commercial hot-food-holding cabinets		X 2006							X 2008			
Commercial prerinse spray valves	X 2008	X 2006					X 2007	X 2007	X 2007		X 2007	1/2006
Commercial refrigerators and freezers	X 2010	X 2003/2006	X 7/2008		X 9/2005	X 2010	X 2010	X 2007	X 2010		X 2007	1/2010
Consumer audio and video products		X 2006/2007					X TBD					Not covered
Digital-television adapters		X 2007					X TBD					Not covered
High-intensity-discharge-lamp ballasts (mercury vapor)									X 2007			1/2008
Illuminated exit signs	X 2008	X 3/2003	X 7/2006		X 3/2005	X 3/2007	X 2007	X 2007	X 2007		X 2007	1/2006
Large packaged ac (more than 20 tons)	X 2010	X 2006/2010	X 7/2009		X 8/2005	X 2010	X 2010		X 2010			1/2010
Low-voltage dry-type transformers	X 2008	X 3/2003	X 7/2006	X 1998	X 3/2005	X 3/2007	X 2003	X 2003	X 2007		X 2007	1/2007
Medium-voltage dry-type transformers				X 2008						X 2008		Not covered
Metal-halide-lamp fixtures	X 2008	X 2006/2008		X 2009			X 2008	X 2008	X 2008	X 2009	X 2008	Not covered
Pool pumps		X 2006/2008										Not covered
Residential furnaces and boilers				X TBD					X TBD	X TBD		Not covered
Residential-furnace fans				X TBD					X TBD	X TBD		Not covered
Single-voltage external power supplies	X 2008	X 1/2007 7/2007 7/2008		X 2008			X TBD	X 2007	X 2008	X 2008	X 2008	Department of Energy rule-making
State-regulated incandescent reflector lamps (BRs, ERs, and R20s)		2008		X 2008			X TBD	X 2007	X 2008	X 2008	X 2007	Not covered
Torchieres	X 2008	X 2003	X 7/2006		X 3/2005	X 3/2007	X 2007	X 2007	X 2007		X 2007	1/2006
Traffic signals (pedestrian)		X 2006					X 2007					1/2006
Traffic signals (vehicular)	X 2008	X 2003	X 7/2006		X 3/2005	X 3/2007	X 2007	X 2007	X 2007		X 2007	1/2006
Unit heaters	X 2008	X 2006	X 7/2006		X 9/2005	X 3/2007	X 2007	X 2007	X 2007		X 2007	8/2008
Walk-in refrigerators and freezers		X 2006							X 2008			
Water dispensers (bottle-type)		X 2006							X 2008			

TBD=to be determined.
X=standard enacted; implementation date as indicated.
Source: The Appliance Awareness Project, updated July 2006.

er supply would operate at 25% power, the efficiency ranges from 58 to 82% (**Figure 3**). Technology is available today to bring that number to more than 90%. Even with each stage's having more than 90% efficiency, the resultant line-to-load or "ac-to-IC" efficiency may be slightly more than 70%: Total efficiency=$(0.9)^3$, or 72%.

The industry has for some time been aware of the challenges that face power-supply designers (**Reference 7**). The DPA (distributed-power architecture) that AT&T developed during the early 1980s is an effective way to convey power from a facility's 240V-ac line to the 1V IC. Unfortunately, it requires several conversion stages.

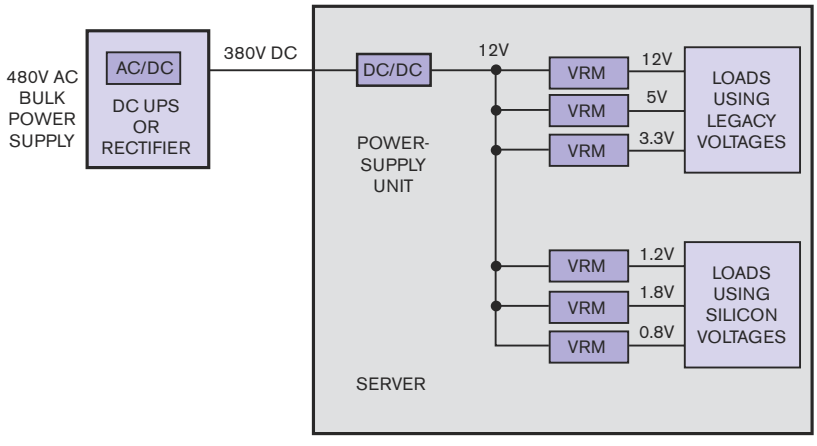
One approach that several leading players in the data-center-equipment business are considering is to use a high-voltage dc-distribution system (**Figure 4**), which could improve the efficiency by as much as 20%. The advocates are enthused about the initial test results that the Lawrence Berkeley National Laboratory at a Sun Microsystems facility achieved this summer. However, the doubters are insisting that there are formidable obstacles to overcome in adopting this architecture. The distribution equipment for high-voltage dc is more expensive and complicated than it is for high-voltage ac. Operating-personnel safety is a great concern—more so than it would be for the equivalent ac power. Expect many animated discussions before participants arrive at a conclusion.

TAKE A POSITION

It is important to discuss energy-efficiency issues with the intention of offering solid solutions. In January 2005, the PSMA (Power Source Manufacturers Association) board of directors issued a policy on power-supply efficiency. It stated that better efficiency was good for users and for the industry. Further, it insisted that manufacturers derive all test procedures and the data gathered to establish standards from processes that include good engineering practices. It also stated that the people and the agencies involved saw improving efficiency as a continuous process, not a single step.

Should improving data-center power-supply efficiency be a mandated or a voluntary process? In a recent meeting, the CEC maintained that it might be better to leave it voluntary. Based on the industry response to being in the hot seat, it looks as though a voluntary approach will solve the problems faster and perhaps more effectively than mandated standards could. However, if that approach becomes stalled, it will open the door for government agencies to step in and complete the process.

Astute marketing and design persons should be well aware of the multiple activities currently going on globally. Further, they should continue to monitor the progress of this work. Industry participants will become involved in the various advisory groups that are feeding industry and market data into the government agencies establishing the standards. Organizations such as PSMA are working to keep members involved in ensuring that the standards the industry adopts are fair and effective. EDN



NOTE: VRM=VOLTAGE-REGULATOR MODULE.

Figure 4 Several leading players in the data-center-equipment business are considering a high-voltage dc-distribution system (courtesy Lawrence Berkeley National Laboratory).

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FOR MORE INFORMATION

You can find a list of relevant vendors and organizations at the Web version of this article at www.edn.com/061109g2.

AUTHOR'S BIOGRAPHY

Arnold Alderman is the agency liaison for the PSMA (Power Sources Manufacturers Association) Energy Efficiency Committee, which advises government agencies globally regarding efficiency standards. Formerly chairman, he continues to be a member of the board of the PSMA, a multinational power-supply-industry association whose members represent more than 50% of the power supplies manufactured globally. Alderman is also founder and president of Anagenesis Inc, a technical-marketing company that focuses on helping companies market their products in the power-conversion and power-semiconductor industries.

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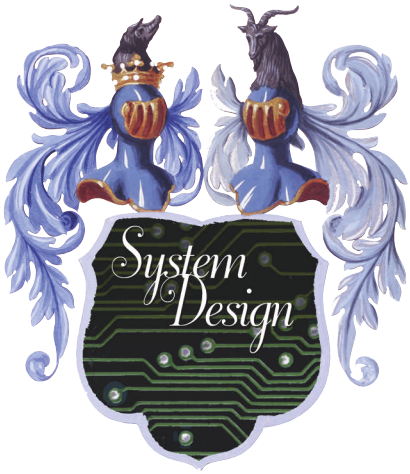

Linux masters the mobile market

BY WARREN WEBB, TECHNICAL EDITOR

Featuring free source code, no licensing fees, and zero per-unit royalties, the Linux operating system has captured the attention of product developers around the globe. To date, Linux has done remarkably well in the Web-server and embedded-systems markets and has built a reputation as a stable, reliable, and crashproof operating system compatible with a wide range of processors. This solid reputation, along with its modular architecture, has also turned Linux into the fastest growing operating system for today's hottest convergence device: the mobile phone.

The growth of Linux in the mobile market has been nothing short of spectacular. Two research companies, Evans Data Corp and The Diffusion Group, both report that by the end of 2005, almost a quarter of all mobile feature phones shipped worldwide were based on the Linux operating system. This phenomenal growth has been mostly at the expense of the market-leading Symbian operating system. Symbian's smart-phone market share had dropped from almost 80% to approximately 50% by the end of last year. To further illustrate the rapid deployment of Linux-based devices, Motorola has suggested that Linux will drive more than 50% of the phones it ships within two years. "Motorola is a firm believer in the power of open platforms and the promise of Linux for mobile," says Greg Besio, Motorola's corporate vice president for mobile-devices software.

Linux market penetration varies depending on location. "The fastest growing Linux volumes are found in Asia, with Panasonic and NEC, and in the United States, with Motorola," says Philippe Robin, ARM's Linux-product manager. "Europe has been slower to adopt Linux due to the domination of Nokia's Symbian operating system." Although these markets are saturated for single-function voice services, Linux allows for increased revenues with new applications and services. New markets are also tempting for Linux developers. For example, The Diffusion Group reports that despite less than 50% coverage today, the entire population of India should be covered by mobile networks by the end of 2009. This additional coverage would extend the number of mobile subscribers from 100 million today to 348 million.

MORE FEATURES, LESS SPACE

You can directly attribute the rise in Linux popularity with designers to the buying public's insatiable appetite for more features in a smaller package. Mobile-phone users are no longer content with a device that has only a single function, so manufacturers must constantly pack more and more features into every new product to compete for market share. In addition to the cellular phone itself, mobile multifunction devices include various combinations of multimedia recorders, players, short-range digital communications, messaging, position-location electronics, and thousands of application programs for work-related information management and personal amusement. With the high volumes and thin profit margins associated with mobile phones, design teams are evaluating and adopting the Linux operating system to tackle the complex software burden.

Linux is modular and allows developers to construct a small, tailored software set that fits the memory footprint of each device, thus eliminating some of the code overhead present in proprietary, multiuse operating systems. Linux also supports a vast arsenal of microprocessors, making it ideal for the diversity of the mobile-phone market. Because Linux has been ported to most popular embedded processors, software limitations don't force developers into hardware decisions. Designers can start production with a low-priced microprocessor that meets current needs and easily upgrade to a more powerful CPU as the device requirements and features expand.

Another Linux advantage is a worldwide team of developers dedicated to chasing down and correcting every internal bug or problem in the kernel. Some of these developers are hobbyists working for nothing, and companies with Linux products support other such developers. Either way, Linux problems get a lot of attention and are usually resolved rapidly. No matter who corrects a bug, the fixes are proposed for incorporation into the next revision of the kernel. Silicon manufacturers also contribute to the open-source community. "Although ARM does not generate revenue from Linux, we have a continuing commitment to support open source," Robin says. "ARM contributes architectural support to the Linux-kernel develop-

IN "POST-MP3" ERA, PORTABLE AUDIO/VIDEO PRODUCTS DIVERSIFY IN CHINA

By Lu Nan, Reporter, EDN China

Profits in the market for basic MP3 players have begun to decline, leading vendors to seek new value-added features that can both spur sales and boost profits. Value-added options include features such as Bluetooth radios and video support. Leading Chinese vendors are considering these and other options.

According to a recent report from GfK, an industry-analyst company, throughout March, April, and May 2006, the Chinese MP3-player market was in a downturn. During that period, the market experienced negative growth, down more than 12% every month. The downturn has led OEMs to become more and more sensitive to BOM (bill-of-materials) costs. And, in seeking new growth opportunities, MP3-chip and -technology vendors must consider new directions in the market. Thus, the "post-MP3" concept is brought to the fore.

Bluetooth support is one trend among the latest player designs, and adding the wireless link is currently a popular practice. Bluetooth can offer value to buyers of MP3 players in two ways. First, Bluetooth can wirelessly connect the player to a stereo headset. Second, Bluetooth can provide a wireless connection to other devices, such as mobile handsets or even PCs.

According to domestic vendors, however, designers face challenges in making the Bluetooth-MP3-player market truly flourish. In the development stage, designers must deal with high cost, inadequate technology maturity, and excessively high power consumption. Currently, the integration of Bluetooth into MP3 players is at a relatively immature stage. Indeed, the IC-design, system-design, and manufacturing phases all must mature for broad deployment. Both design capability and design cost are affecting the promotion of Bluetooth-enabled MP3 players.

In addition to adding Bluetooth functions to MP3 players, domestic vendors are divided as to which functions products in the post-MP3 age should have. According to Zhuhai Action, the largest MP3-chip vendor in China, post-MP3 products will come in four basic flavors:

- **Basic, audio-only MP3 players;**
- **Small-screen, video-capable devices based on proprietary video technology;**
- **More capable MPEG-4, H.264 video players; and**
- **Multiformat PMPs (portable media players) with a hardware codec.**

In 2006 in the Chinese market, according to Zhuhai Action, the four product types will respectively account for 88, 7, 4, and 1% of the total market. In 2007, these percentages will evolve to 70, 16, 13, and 1%, respectively. Clearly, products in the small-screen and MPEG-4 categories will grow rapidly.

Auview Technology, a multimedia-equipment vendor in China, plans to focus its offerings on these two categories this year and next year. After introducing products in the small-screen-system to the market this year, Zhuhai Action will focus on its MIPS+DSP ATJ213X series chip, targeting the MPEG-4-video-player market.

Small-screen and MPEG-4 post-MP3 products also give opportunities for leading vendors of 8-bit microcontrollers to join the game. Atmel, for example, has been active this year. Lin Liangjun, general manager of Atmel in China, would like the industry to regard Atmel as a multimedia-processor vendor, because Atmel's new products in the Chinese market indeed aim at multimedia applications. Atmel will also target small-screen and MPEG-4 devices with embedded processors featuring diversified multimedia capabilities.

Many domestic vendors also believe that the needed innovations in post-MP3 products will include display technologies. Increasingly robust video-playing functions demand larger and higher resolution displays. Screen size, color performance, and resolution need to improve, which will afford great business opportunities for flat-panel-display vendors.

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TRENDS SHAPING THE FPGA INDUSTRY

By Denice Cabel, Group Online Editor, EDN Asia

FPGAs continue to penetrate new markets and increasingly serve as the heart of electronics systems. The value of worldwide FPGA shipments will increase from $1.9 billion in 2005 to $2.75 billion by 2010, according to In-Stat. Much of this revenue will come from low-volume shipments. The largest end-use segments will be communications and industrial.

The market strength of FPGAs arises from two factors: They provide higher density and performance than alternative PLDs (programmable-logic devices), allowing them to implement more functions, and the cost of alternatives, such as ASICs and ASSPs, is in many cases too high to justify their development.

According to a study that AG Edwards & Sons Inc conducted, two trends are developing in the FPGA market. First, flash-memory-based FPGAs are showing visible gains, with designs using them expected to climb by 44%. Second, FPGA users are looking for processor-agnostic design approaches that allow them to use third-party IP (intellectual property), such as ARM and MIPS processors.

Altera and Xilinx still lead in the programmable-logic industry, controlling 84% of the market. That scenario leaves the six other established companies–Actel, Atmel, Cypress Semiconductor, Lattice Semiconductor, and Quicklogic–plus a few other PLD players, to compete for the remaining 16% of the market.

PLD GROWTH IN ASIA

Cheng Hing-Nan, marketing director of Xilinx Asia-Pacific, cites wireless communications as the first of three growth areas for the PLD industry. This situation arises from the strength of the cell-phone market, particularly in China and India, where new infrastructure equipment will also be necessary.

The second area of tremendous growth potential lies in wired communications, specifically in FTTH (fiber-to-the-home) applications. "In Japan, the number of FTTH subscribers has surpassed new DSL subscribers," Cheng says.

The third strong market for PLDs is the digital consumer market. "More consumers are replacing their current televisions with HDTVs and flat-panel displays," Cheng says. "In addition, broadcasters and studios will need to replace and upgrade their transmission equipment to meet the demand."

Systems designed in Asia do not significantly differ, in quality, from systems in similar applications developed elsewhere, Cheng says. Engineers in Asia are as skillful as their peers in other regions, so there are no differences in usage.

Moreover, the common perception that Asian engineers use predominantly low-density devices because their companies produce only consumer devices is incorrect. "It is true that many consumer products use low-cost FPGAs but not just consumer products," says Cheng. "In every electronics market, lower cost systems are usually sold at higher volumes than high-end systems."

KEY FPGA INNOVATIONS

As the FPGA industry moves to 65-nm-process technology, power consumption is becoming a key consideration, says Danny Biran, vice president of product and corporate marketing at Altera. Keeping low power consumption and increasing density and performance are key areas of innovation.

In addition, design software is becoming a critical part of the FPGA's value. "As devices become more complex, FPGA-design software needs to address challenges that in the past only existed in the ASIC space, such as timing closure, power closure, and system-level design," Biran says. "Customers increasingly look for a migration path from FPGA to low-cost structured ASIC for volume production. For volumes of tens of thousands to hundreds of thousands of units, structured ASICs offer a low-cost solution at a much lower cost and much faster time to market than standard-cell ASICs."

Another continuing trend is the infusion of FPGA hardware into the embedded-systems community and the general convergence of hardware platforms. Industry trends are pushing FPGAs, structured ASICs, DSPs, and conventional processors toward some virtual point of convergence. FPGAs started as almost purely programmable fabric but have since added embedded processor cores, memory, sophisticated I/O capabilities, hard-wired multipliers, and dedicated peripherals to increase their versatility as embedded platforms. On the other hand, structured ASICs look almost identical to FPGAs in their hard-IP offering, differing only in the programming method for the configurable fabric.

Electronics manufacturers must meet their customers' needs by developing more complex products without increasing R&D budgets, without increasing design risk, and while reducing time to market. All of these requirements favor the use of programmable logic over ASICs.

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ment, promotes standardization initiatives, and provides early access to technology to promote adoption by the open-source community." ARM also maintains a Linux Wiki (www.linux-arm.org) for the latest developer information.

Linus Torvalds first released Linux in October 1991, and he remains its author and trademark holder. The basic architecture of the Linux kernel includes memory management, process scheduling, a file system, and a communications interface. The memory manager enables multiple programs to securely share the system memory, and the process scheduler ensures that programs have fair access to the CPU. The virtual file system hides the details of the hardware and presents a common file interface to the developer. The Linux kernel updates periodically to include patches and suggestions from the user community. You can find information on and download the latest version of the kernel at www.kernel.org.

CONTROLLING PATCHES

One possible danger that mobile-phone vendors foresee in an open-source Linux environment is the potential for fragmentation. If a developer modifies the Linux kernel to solve an integration problem, that action creates two different and possibly incompatible versions of Linux. When the next official Linux update comes out, the developer will have to search through the revised code to reincorporate the modifications or continue to use the old version. So far, the Linux community has been successful in preventing multiple versions through an elaborate system of upgrade proposals and releases.

MULTINATIONAL TEAMS FORM IN JAPAN TO ADDRESS BURGEONING GLOBAL-HANDSET MARKET

***By Ken Amemoto, Senior Editor, and Takatsuna Mamoto, Editor in Chief,* EDN Japan**

Japanese handset makers have fared well in the domestic market and, in fact, have been technology leaders in 3G handsets for NTT DoCoMo. However, the same vendors haven't succeeded nearly so well globally or in the still-growing 2G market.

To boost their worldwide presence, Japan's handset vendors are teaming with other handset vendors, chip vendors, and service providers. Two heavyweight groups have emerged. One includes NEC, Panasonic, and Texas Instruments, and the other features Renesas Technology, Fujitsu, Mitsubishi Electric, Sharp, and NTT DoCoMo.

NEC, NEC Electronics, Matsushita Electric Industrial, Panasonic Mobile Communications, and Texas Instruments have formed a new joint company called Adcore-Tech to develop a 3.5G platform that includes hardware and software, as well as to study "3.9G" systems–those close to 4G in functions but based on underlying 3G technologies.

The new company plans to provide an enhanced communication platform to domestic and global markets, in the latter case filling the global void for the Japanese handset companies. The partner companies have compelling assets. The NEC and Panasonic Groups have established 3G technologies, and TI brings its GSM (Global System for Mobile communications) expertise in the 2G/2.5G market. The joint venture aims to win 20% of the global communication-platform market.

Adcore-Tech will license the technology it develops to NEC and Panasonic. The five founding companies will provide funding and development resources to Adcore-Tech, and Adcore-Tech will develop a post-3G technology platform. Adcore-Tech will license 2.5G and post-3G design data to NEC Electronics, Matsushita Electric Semiconductor, and TI. NEC and Panasonic Mobile will produce handsets integrating the licensed chips. NEC Electronics, Matsushita Semiconductor, and TI will be able to sell the chips to other cell-phone manufacturers. Adcore-Tech will license the mobile-communication-platform technology, including software for smart phones, system-evaluation services, and customized services, to cell-phone manufacturers.

The investment in Adcore-Tech totals 1.2 billion yen (about $100 million): 44% from the NEC Group, 44% from the Matsushita Group, and 12% from TI.

Meanwhile, the Renesas-led group hopes to win global business with a platform based on the SH-Mobile G series single-chip and basic software. The partners plan to develop the platform by the second quarter of 2007. Following SH-Mobile G1 products that have been mass-produced since the second quarter of 2006, the SH-Mobile G2 now under development is now available for sampling. The latest chip integrates a baseband processor that supports up to 3.6-Mbps HSDPA (High Speed Downlink Packet Access) and EDGE (Enhanced Data rates for GSM Evolution) standards, along with the capabilities of the earlier G1 baseband. Mass production will commence in the third quarter of 2007 using a 65-nm process.

Renesas will provide handset OEMs with a platform including an OS, driver software, communication-control software, and middleware, as well as the chip. The platform relies on the Symbian OS along with FOMA (NTT's 3G format) software, which NTT DoCoMo developed. The group will support Linux in the future.

Renesas will use a system-on-chip development platform called EXREAL to develop the SH-Mobile chips. The platform reportedly helps design engineers shorten the development period by as much as 40%, as well as promotes reuse of software resources.

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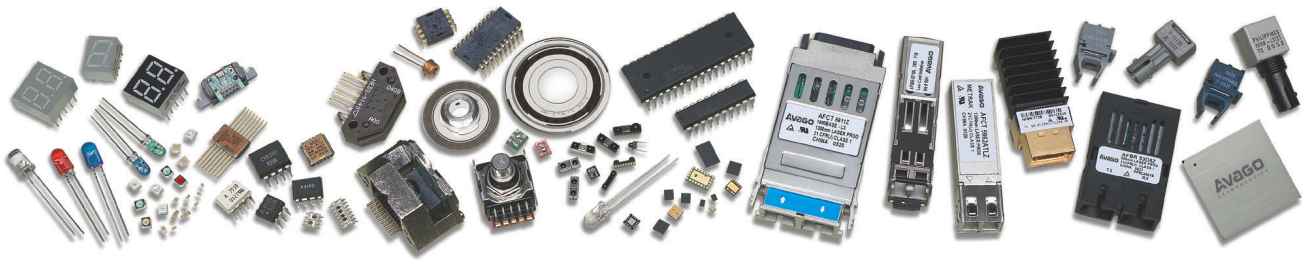

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Mobile-phone software also has unique requirements that the Linux kernel does not address. For example, the user interface is undefined, although multiple open-source implementations are available to designers. Mobile operating software may also need power management, reduced boot-up time, and possible real-time operation. Call-management and data-communications routines are extremely important in a mobile-phone environment but are as yet unavailable as open-source components.

The Linux Phone Standards (LiPS) Forum and the Open Source Development Labs (OSDL) have recently teamed up to address these deficiencies and define standards that promise to turn Linux into a plug-and-play mobile-phone platform. Motorola, NEC, NTT DoCoMo, Panasonic Mobile Communications, Samsung Electronics, and Vodafone recently announced plans to work toward a global, open, Linux-based software platform for mobile devices. They hope to provide an API (application-programming-interface) specification, architecture, open-source code, rules for third-party software, and a conformance test suite.

The Linux licensing agreement has positive and sometimes negative consequences in the highly competitive mobile market. On the positive side, you can download a free copy of Linux, adapt it to your product, and sell as many units as you want without paying royalties. Yet Linux is not public-domain software; it is licensed under the GNU General Public License (GPL), which contains specific rules for its use. If you modify and distribute GPL software, your modifications automatically fall under the GPL, and you must give the source code to anyone who asks for it. Your application programs and device drivers may remain proprietary as long as they are separate and distinct from the Linux kernel and contain no GPL code. This code isolation is a constant source of anxiety among developers, especially in small-footprint mobile systems in which all software links together in a single ROM image.

FREE SOFTWARE REVENUE

With the software available for free, Linux vendors have adopted multiple business models to ensure sustained revenue. Some vendors offer product-development or consulting services, and others offer telephone-support services similar to those that traditional operating-system suppliers provide. Still others have packaged Linux and their own proprietary add-ons or development tools into a distribution disk for sale to designers. For example, MontaVista offers the Linux for Mobile Devices (Mobilinux) operating system for wireless handsets and mobile products with requirements for power management, hard real-time performance, fast start-up, and a small footprint. Simi-

CHINESE MOBILE-PHONE VENDORS VACILLATE ON OPERATING-SYSTEM STRATEGIES

***By Zhou Xin, Technical Editor,* EDN China**

Symbian's expensive license makes Chinese mobile-phone vendors flinch. The wireless connection between Windows Mobile and PC applications seems promising. The Linux kernel is free, but mobile-phone vendors are still unwilling to use it as the foundation of their operating systems.

Like their counterparts elsewhere, mobile-phone vendors in the Chinese market face a quandary when selecting an operating-system platform. They hope to effectively develop next-generation smart mobile phones with proprietary intellectual property, but they have not yet made a clear selection among Symbian, Windows Mobile, and Linux.

Among the several prevalent operating systems, Symbian has long had a strong advocate: mobile-phone giant Nokia. In addition, Microsoft recently reached an agreement with Symbian to open synchronous software functions, dramatically improving the interoperability between Symbian and PC systems. Nonetheless, Symbian now faces a problem in China: It seems that no homegrown mobile-phone vendors are willing to use its products. The mobile phone is a cost-sensitive product in the Chinese market, and, according to these vendors, the use of Symbian's products adds significant royalties, increasing their design cost and putting them at a disadvantage in the market.

Microsoft's Windows Mobile system targets higher end smart-phone products. In addition to its good technical capabilities, its unique advantages lie in the recognition that PC users give to Windows. This year, Microsoft has been promoting a vision of "seamless" connections and shared resources. As PC-based Windows has gained a large share of the Chinese market, the interconnection and interoperability between mobile devices and PCs will help improve opportunities for Windows Mobile.

European vendors perceived the Linux kernel as a good match for mobile-phone designs for the Chinese market. But it turns out that China's design community has problems with Linux. Although Linux is an open kernel, development of mobile-phone systems based on such a kernel is not cheap. Only the kernel is free; costs for R&D, testing, optimization, and integration actually run quite high, and the development cycle is very long.

Moreover, the limited number of Linux-based applications also constrains the operating system's penetration in the mobile market. Finally, different versions of Linux come with diversified libraries and SDKs (software-development kits). These variants don't provide the consistent platform that phone-design teams need.

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larly, PalmSource recently revealed details of its Linux-based mobile-phone operating system, which can run legacy Palm OS application binaries, Java applications, and native Linux applications. Norway-based Trolltech has also announced a hardware-reference design and custom Linux distribution for mobile phones. And finally, Wind River Systems, supplier of the popular VxWorks real-time operating system, has launched the Platform for Consumer Electronics, Linux Edition, which targets mobile phones, set-top boxes, personal video recorders, and other small-footprint consumer-electronics devices.

Although Linux may not yet be the perfect operating system for every mobile-phone application, it has enough built-in features and future promise to lure scores of phone developers into its camp. Developers can go it alone or select commercial vendors providing custom software distributions, subscription support packages, development tool kits, and reference designs to augment the free Linux core. With these benefits and a worldwide army of developers ready to resolve integration issues, Linux has a bright future in the mobile-phone industry.EDN

FOR MORE INFORMATION

You can find a list of relevant vendors and organizations at the Web version of this article at www.edn.com/061109g1.hhI

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MEMORY OPTIONS: FLASH MAY DOMINATE

By Kenji Tsuda, Editorial Director, EDN Japan

Microcontrollers that integrate flash memory are beginning to flood the market, bringing with them advantages for engineers.

For example, NEC Electronics reports that shipments of flash-based microcontrollers grew 29.6% in fiscal 2005 and will grow 91.4% in fiscal 2006. Renesas Technology also reports significant growth; the company shipped 700 million units from 2001 to June 2005 and expects to reach 1 billion units by March 2007. Fujitsu, Toshiba, and Panasonic also offer flash-based devices, and the trend extends beyond the Japanese vendors, with Freescale Semiconductor, STMicroelectronics, Atmel, and others also strengthening their flash-based offerings.

Flash microcontrollers offer a number of advantages centered on programmability. You can program the devices before or after mounting on a pc board and before or after shipment into the market. Flash microcontrollers, however, have been 20 to 30% more expensive than conventional mask-ROM or OTP (one-time-programmable) ROM versions. The cost premium resulted in IC vendors offering fewer families and derivatives relative to the other product types.

So what has prompted the recent expansion in the flash-microcontroller market? Certainly, a shrinking cost premium for flash is partly responsible. But designers also value the flexibility and shorter time to market that flash-based devices can deliver. In addition, a growing set of development tools from third parties supports quicker design cycles.

Semiconductor process technology also is swinging in the favor of flash. Compared with past devices, today's microcontrollers feature greatly increased transistor density, which allows the integration of broad sets of peripherals. The die area dedicated to memory is shrinking relative to the other functions. Though mask-ROM-based devices were once easier to produce, that advantage has shrunk considerably.

In the current era, when manufacturers offer a wide variety of OEM products with relatively small manufacturing volumes, programmable microcontrollers prove the best choice for many manufacturers. Both the manufacturer and the IC vendor can program the devices. The turnaround time is effectively zero: OEM manufacturers don't have to wait for the mask-program step.

Chip vendors also enjoy many advantages. They can produce flash-microcontroller products in increasing volumes and reduce the price premium. And when OEM customers cease production of a particular product, the IC vendors aren't left with unusable inventory.

Flash devices may also be more reliable than mask-ROM devices. According to one OEM, the first mask-ROM products produced for a new design sometimes exhibited insufficient noise immunity–a severe problem that could result in a revision in the design. Meanwhile, a vendor ships the same proven flash-based designs to every OEM customer.

Renesas recently reviewed its flash-microcontroller strategy. The company had already developed a family of flash microcontrollers branded Z-TAT (zero turnaround time). The Renesas portfolio, however, includes a variety of microcontrollers that integrate flash memory, OTP memory, and mask ROM–targeting architectures to specific applications. Like NEC, Fujitsu is shifting to focus on flash microcontrollers, moving away from conventional OTP and mask-ROM products.

OEM designers may also see further reduction in flash-microcontroller prices, driven by new players with their own IP (intellectual property). Upstarts such as Impinj from the United States and e-Memory of Taiwan are entering the market. The Impinj Flash IP features no additional mask steps, whether targeting microcontrollers, LCD drivers, or electronic-ID applications. The Impinj IP design, however, is suitable only for relatively low-density, 2- or 4-kbit products. The e-Memory IP requires just three masks but delivers 2-Mbit or higher density flash that you can integrate on a microcontroller chip. Renesas has licensed the e-Memory IP.

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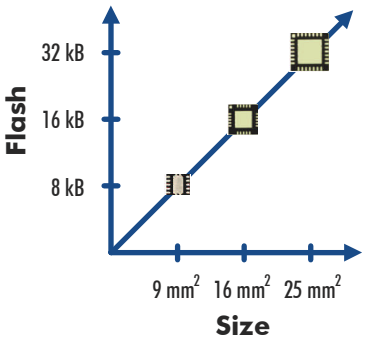

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ANALOG IS THE REAL WORLD, AND NEEDS DIFFER FROM PLACE TO PLACE. ACCORDINGLY, ANALOG ENGINEERS FACE CHALLENGES IN ACCOUNTING FOR A MULTIPLICITY OF STANDARDS, CONVENTIONS, AND CONSUMER PREFERENCES, DEPENDING ON WHERE A PRODUCT FINDS USE.

Globalization and analog

BY PAUL RAKO, TECHNICAL EDITOR

The requirements of globalization often impact analog-system designers more than they do other designers because analog is the interface to the real world. That world changes from country to country and from culture to culture. The old phone system was one of the few systems that had some uniformity all over the world. In television, Europe has PAL (phase-alternation line), and the United States and Japan have NTSC (National Television System Committee). High-definition-TV standards remain unsettled, as content owners, such as the major studios, try to force hardware manufacturers to adopt DRM (digital-rights-management) schemes.

Cell phones operate on four frequencies and have both analog and digital protocols, and many frequency and modulation standards exist for wireless and phone protocols (**Reference 1**). Analog designers rose to the challenge with triband or even quadband phones that work in many areas. "One of the big challenges in designing wireless products for global markets relates to the regional differences in frequency allocations," says Doug Grant, director of business development, RF, and wireless systems at Analog Devices. "For example, the frequency bands for the GSM [Global System for Mobile communications] cellular system in North America are 850 and 1900 MHz, whereas, in the rest of the world, they are 900 and 1800 MHz. The bands are far enough apart that [manufacturers have to optimize] matching networks for each of the four bands." He also notes that, when developers were first contemplating 3G cellular, they hoped that a single air interface for use in a limited number of bands would emerge. "Somehow, over time, we've lost the U in UMTS [Universal Mobile Telecommunications System] and have multiple air interfaces and multiple frequency bands. In other applications, such as short-range, unlicensed wireless links, the frequency allocations differ, and the specs for transmitter-signal purity vary widely because different services are in the adjacent bands in each region," he says.

Hardware engineers have also come to the aid of consumers when manufacturers have patented protocols, such as CD-R, CD+R, and the rewritable DVD formats. Engineers simply created drives that would support all the formats. The high-definition-DVD conflict will be even more difficult, because the HD-DVD and Blu-ray camps are vying for dominance, and China announced it would conform to neither standard and issued a proposal for a disk based on its EVD (enhanced-versatile-disc) standard. Once the bits on a DVD get past the read channel, digital engineers all have similar jobs. Analog engineers, on the other hand, must provide the laser drivers, the read-channel signal chain,

and the servo system to track the disk as those digital bits come pouring out.

Analog designers also face issues of global regulatory compliance. In the United States, they must comply with the UL (Underwriters Laboratories) listing, and, in Europe, they must comply with the CE (Conformité Européenne) standard. FCC (Federal Communications Commission) standards determine RFI/EMI (radio-frequency-interference/electromagnetic-interference) emissions in the United States. In Europe, CE details not only RF emissions but also RF immunity. These immunity standards have proved more challenging than the emissions standards for engineers to meet. The Crown Audio Web site lists the following CE standards that its products are subject to for US and Canadian standards. Crown also must comply with worldwide standard if they want to sell their products internationally (**Reference 2**).

- EN 55103-1: 1995 Electromagnetic Compatibility Product Family Standard for Audio, Video, Audio-Visual, and Entertainment Lighting Control Apparatus for Professional Use, Part 1: Emissions;
- EN 61000-3-2: 1995+A14: 2000 Limits for Harmonic Current Emissions (equipment input current≤16A per phase);
- EN 61000-3-3: 1995 Limitation of Voltage Fluctuations and Flicker in Low-Voltage Supply Systems Rated Current≤16A;
- EN 55103-2: 1996 Electromagnetic Compatibility Product Family Standard for Audio, Video, Audio-Visual, and Entertainment Lighting Control Apparatus for Professional Use, Part 2: Immunity;
- EN 61000-4-2: 1995 Electrostatic Discharge Immunity (Environment E2-Criteria B, 4 kV Contact, 8 kV Air Discharge); and
- EN 60065: 1998 Safety Requirements Audio Video and Similar Electronic Apparatus.

To illustrate just how complex it can be for analog designers to span these differences, consider something really simple, such as plugging a device into an outlet: Even this task can be daunting for an analog engineer.

POWER GLOBALIZATION

One obvious problem that analog engineers face is the diversity of ac-power standards. The US Department of Commerce publishes the 30-pg *Electric Current Abroad* (**Figure 1**), which details not only worldwide voltage and frequencies of ac power, but also the plugs and receptacles in use (**Reference 3**). The IBM division that sells its mainframe-computer power front end to industrial customers offers an internal document that shows the power quality of the ac power in all countries. The spikes, sags, and frequency variations can be even more difficult to design for. A universal supply is universal in name only if it can operate from 90 to 240V on 50 or 60 cycles. That supply must also withstand the stresses of surges and spikes. A savvy designer also must understand that many countries often experience dropouts of two or even five cycles, so designers must use higher value input-holdup capacitors than they would normally use.

"To compete in the global market, today's analog ICs must address a wide range of application and voltage requirements," says Doug Bailey, vice president of marketing for Power Integrations. "For example, we know that Japan's ac main can be as low as 90V power, whereas Europe uses 240V. At first blush, this information seems like enough to design a power supply that will operate worldwide. The reality is more difficult. In India, the power grid is unreliable, forcing many big electricity consumers to use private generators during outages. When the power goes down, and the generators switch in, numerous line spikes occur. When the power grid comes back up, everyone's using generators. The power grid is unloaded, so the voltage can overshoot and ring for several minutes. The resulting surges can go as high as 400V. Products have to be able to handle these extremes, so our application circuits must cover ultrawide ranges of voltage and help ensure that our chips withstand the spikes."

Besides fundamental voltage differences, analog-system designers must consider regulatory differences on power supplies. In Europe, the IEC (International Electrotechnical Commission)

Country or city	Type and frequency of current	Number of phases	Nominal voltage	Number of wires	Frequency stable enough for electric clocks?
Brunei[1,2]	a.c. 50	1, 3	240/415	2, 4	yes
Bulgaria	a.c. 50	1, 3	220/380	2, 4	no
Burkina Faso	a.c. 50	1, 3	220/380	2, 4	no
Burma[1,2,3]	a.c. 50	1, 3	230/400	2, 4	no
Burundi[3]	a.c. 50	1, 3	220/380	2, 4	no
Cambodia	a.c. 50	1, 3	220/380	2, 3, 4	no
Cameroon	a.c. 50	1, 3	220/380	2, 4	yes
Canada[1]	a.c. 60	1, 3	120/240	3, 4	yes
		1, 3	220/380	2, 3, 4	no

Figure 1 *Electric Current Abroad* details the differences in ac-power needs worldwide.

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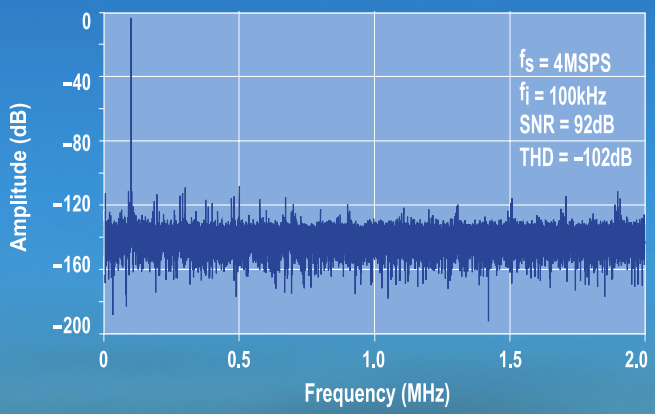

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standard 61000-3-2 took effect in 2001. China and Japan have adopted similar legislation. This standard applies to power supplies of more than 75W. In those cases, the law prevents creating input harmonics over a small level. This requirement effectively mandates a power-factor-correction circuit. In a conventional line-power-supply front end, once the capacitor charges up at turn-on, the only current that flows into the capacitor is at the peak of the input-voltage waveform (**Figure 2**). These current spikes mean that the input current does not track the input voltage—that is, the input current is not a sine wave. For countries that mandate low input harmonics, the supply has to use a power-factor-correction front end (**Figure 3**). This configuration uses a boost topology that uses the input-sine-wave voltage as a reference for the input current. This reference results in a dc-output voltage about twice the peak input but ensures that few harmonics inject themselves back into the power gird.

Harmonic regulations represent just one aspect of worldwide power regulations. A global designer must take into account many other standards, such as the US Energy Star program for computers, and regulations that limit the amount of standby power that remote-control circuits, such as IR detectors, use. In California, the cost of electric power is about $1/W for a device that runs 24 hours a day, seven days a week, all year. If your house has many standby remote-control circuits, it may cost more than $100/year just to keep them on and ready for your command. Several jurisdictions around the world are acting to limit the amount of power standby circuits use. Power Integrations has a table of them on its Web site under "Green Solutions/Regulations" (**Reference 4**).

Globalization presents challenges to other aspects of power supplies besides ac power. Global markets have needs that will require special features in handheld products, such as cell phones and MP3 players. A standard reference design will provide for the powering of

EVALUATE, SIMULATE, AND PROTOTYPE 24/7 WITH THE WEB

By Dave Kress, Analog Devices

Although one could argue that the advent of the Web has reduced interpersonal interaction, it has had undeniably positive effects on many aspects of technology design and manufacture. While many people immerse themselves in online gaming or spend hours bidding on coveted eBay items, design engineers are using the Internet to save valuable time on their next-generation designs. Indeed, the need to provide worldwide design support 24/7 has long since inspired semiconductor suppliers to adopt the Web as a vital link to engineers. So let's examine how the Web has benefited the design process.

What started off essentially as an electronic repository for data sheets and application notes soon evolved to include parametric search engines that made finding the right product faster and easier. More recently, Web-based tools have begun providing real-time design support and troubleshooting tips that are saving designers the time and hassle of requesting hard-copy data sheets, samples, and evaluation boards over the telephone and then waiting–for weeks in some cases–to receive them. The era of passive online data warehousing has given way to an age where "always-on" support and intelligent tools are key differentiators for component suppliers in their quest to deliver value and customer satisfaction.

So how do online development tools accelerate time to market and optimize design resources? First, they help designers make the best selection possible from among the hundreds of products typically available in each component category. Take amplifiers, for instance. How do you find the right one for your design? Enhanced parametric search engines represent one option, but semiconductor companies have taken such conventional searches a step further.

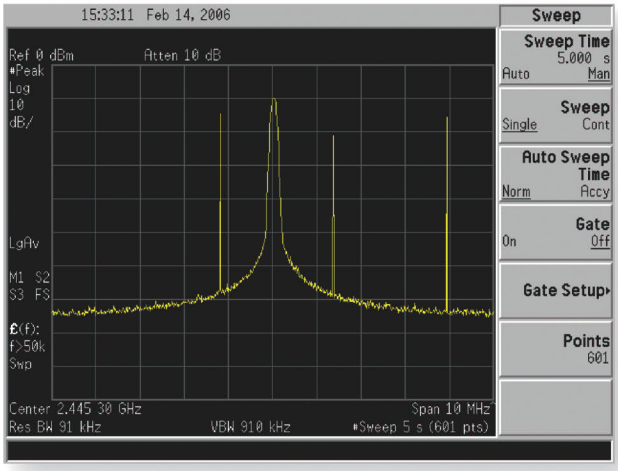
System engineers now have access to free, online evaluation tools that not only winnow the component catalog, but also use parametric data to mathematically model the general behavior of the selected IC, virtually configure it within the system or subsystem design, and apply a signal to evaluate the product's general performance. This step reduces tedious hand calculations and removes much of the guesswork from the selection and evaluation process. As a result, engineers can quickly and efficiently conduct real-time simulations and troubleshoot potential problems across various parameters and architectures. Once he has selected the part, the designer retains a blueprint of the circuit–including detailed information on potential system errors and dynamic performance–thereby further simplifying the design process.

Designers also have access to another Web-based option, a continuously evolving online catalog of system configurations. Because these aim to interact with designers, such configurations provide options for building a complete signal chain and can even communicate the component requirements. In many cases, such detailed information allows designers to generate a schematic from which to start the design, a process that is a lot more convenient and effective than beginning with a blank sheet of paper.

The Web will continue to assist in the design process, and, to keep up with the ever-changing nature of technology, it will need to continue evolving. The industry will expect semiconductor companies to usher in these advancements, and these companies will need to work closely with designers to determine next-generation needs.

AUTHOR'S BIOGRAPHY

Dave Kress is the director of applications engineering at Analog Devices (www.analog.com).



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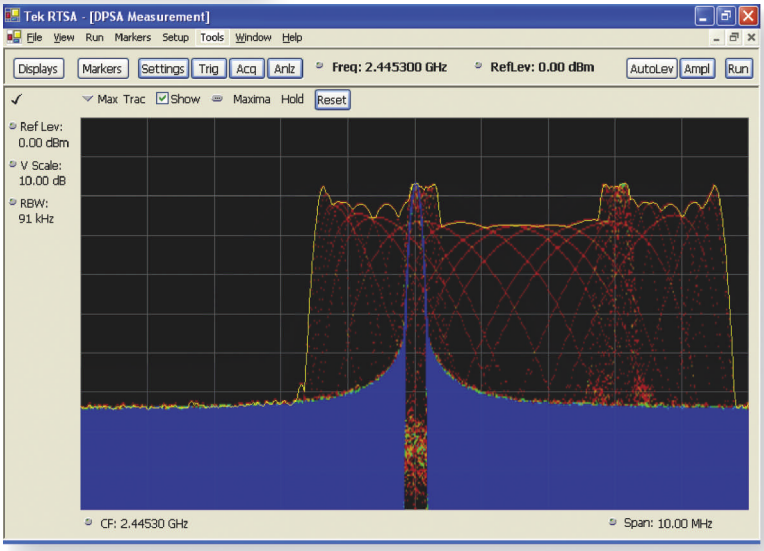

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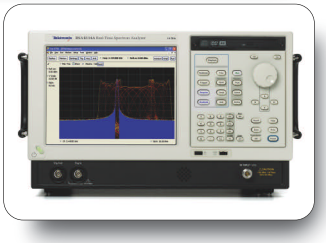

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THE REGULATORY CHALLENGE TO WIRELESS EMBEDDED CONTROL

By Sherif Hanna, Cypress Semiconductor Corp

Most of us have used short-range-wireless technologies in the form of point-to-point Bluetooth connectivity between mobile phones and headsets or between a PC and a wireless mouse. Short-range-wireless technologies typically have a range of 10 to 50m and data rates of less than 4 Mbps. These technologies enable a new concept, WiEC (Wireless Embedded Control). The philosophy of WiEC calls for the ubiquitous embedding of simple wireless transceivers in host systems beyond PC peripherals and consumer electronics. You can use these transceivers to report data or receive commands, creating networks out of otherwise-standalone machines. You can then use these networks to enhance the performance and the efficiency of member nodes.

WiEC-friendly transceivers vary based on data rate, range, occupied bandwidth, collocation ability, and immunity to interference. Local agency regulations for the transceiver band in which the transceiver operates directly impact some of these properties. Therefore, the choice of frequency band affects system performance. A wireless system may operate in a licensed or an unlicensed frequency band. Licensed bands have the advantage of guaranteeing a slice of spectrum dedicated to the wireless system, thus reducing the possibility of interference. However, licensing costs and regulatory certification procedures can significantly increase costs and time to market. Unlicensed frequency bands offer an alternative, but with a caveat. A wireless system can operate in an unlicensed band as long as it complies with restrictions on power output, spectral density, and duty cycle and simultaneously accepts potential interference from other devices in the same band.

But unlicensed bands are not all the same. Typically, the higher the center frequency of the band, the wider the band itself and, thus, the more devices it can accommodate. Conversely, free-space propagation of lower frequencies is typically better than that of higher frequencies, implying that a lower frequency wireless transceiver would have more range for a given RF output power.

The center frequency and bandwidth of unlicensed bands vary by local regulatory agency, which can cause headaches for companies that want to sell a product globally. But the 2.4-GHz ISM (industrial/scientific/medical) band is unique in that most regulatory bodies worldwide have adopted a center frequency of approximately 2450 MHz and bandwidth with sufficient overlap to allow for relatively easy global deployment. This adoption has had the positive effect of the proliferation of consumer and WiEC-type wireless devices but has caused severe spectrum crowding.

Nonetheless, because of international availability, bandwidth, and simplified regulatory requirements, the 2.4-GHz ISM band is possibly the most suited to WiEC applications. But this suitability presents a challenge to WiEC-type transceivers, because they must be able to coexist in a crowded spectrum. Wireless devices that inhabit the same unlicensed bands as WiEC devices provide two challenges. First, they may occupy more bandwidth than a WiEC-type transceiver and thus consume spectrum that WiEC networks can otherwise occupy. For example, an IEEE 802.11g access point occupies 22 MHz of spectrum, compared with a WiEC-type transceiver, which typically occupies 5 MHz or less. Second, these other wireless devices can be of much higher RF output power than a low-power WiEC transceiver, thus interfering with WiEC networks operating in nearby frequencies. For example, IEEE 802.11g access points can have power outputs as much as 100 times those of a typical WiEC transceiver.

Therefore, a WiEC transceiver must employ effective interference avoidance, including the ability to detect RF energy on a frequency, to recover from transmission errors, to provide automatic acknowledgment and retransmission, and to possibly provide spread-spectrum modulation. Furthermore, a WiEC transceiver must occupy minimal spectrum, thus enabling it to find a clear communication channel even in a busy RF environment.

Collocation poses another challenge. For WiEC to realize its full potential, the underlying radio technology must enable a large number of nodes to operate simultaneously. This ability is critical for applications such as environmental control in large buildings, inventory tracking in warehouses, and appliance control in dense housing units. A WiEC transceiver that occupies a small operating bandwidth would be appropriate because it would increase frequency diversity and possibly enable dozens of nodes to collocate in close proximity. A better transceiver would also employ some form of code diversity, as in the case of DSSS (direct-sequence-spread-spectrum) modulation, which can raise the number of collocatable nodes to hundreds instead of dozens.

We all stand to benefit from the added intelligence WiEC will bring to familiar systems. The challenge to system designers lies in selecting an underlying transceiver technology that will be easy to design in and to deploy globally.

AUTHOR'S BIOGRAPHY

Sherif Hanna is a member of the strategic-marketing team for Cypress Semiconductor's wireless products.

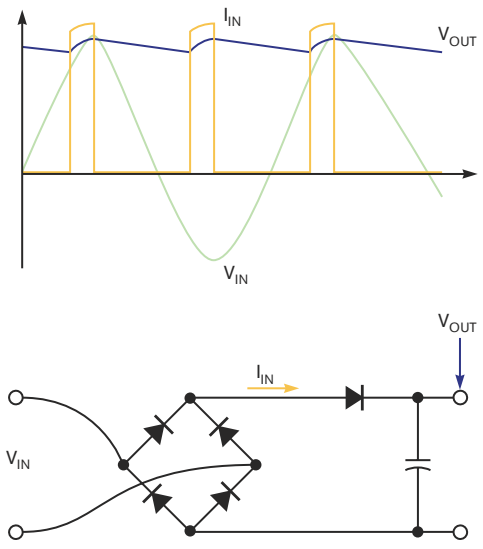


Figure 2 A conventional power-supply front end has large current spikes and poor power factor.

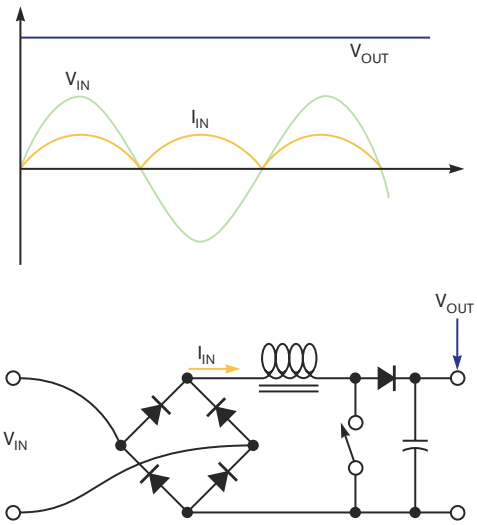


Figure 3 A PFC front end uses a boost converter to ensure that the input current is a sine wave rather than a series of pulses.

a base system. But if a market requires multiple cameras or colored-LED lighting that flashes in time with music, then the power system will become far more complex. In addition, some countries may have requirements that dictate the use of certain battery chemistries.

"As far as globalization's effect on our customer's power requirements, there is less of an impact for the handheld-system market," says Roger Woodward, western regional sales manager at Summit Microelectronics. "The battery for a portable player or cell phone is the same in Japan as it is in the United States or in India. We do see an impact on the local market requirements for features. When a market demands more features, that demand requires specialized power chips." He says that one benefit of digitally controlled analog-power systems is that they build programmability and control of the power system into the chip.

Summit does not develop digital-power chips in the sense of using a DSP to control the loop. "Our customers make handheld, battery-powered products. The first question they ask is: 'How high is the quiescent current?' If we told them anything more than 50 µA, they would not even want to see a data sheet and would not ask us back," says Abid Hussain, Summit Microelectronics' director of marketing. "We cannot have a DSP closing the loop and drawing milliamperes of power. That is why we discourage the term 'digital power' in reference to our products. We prefer 'digitally controlled analog.'"

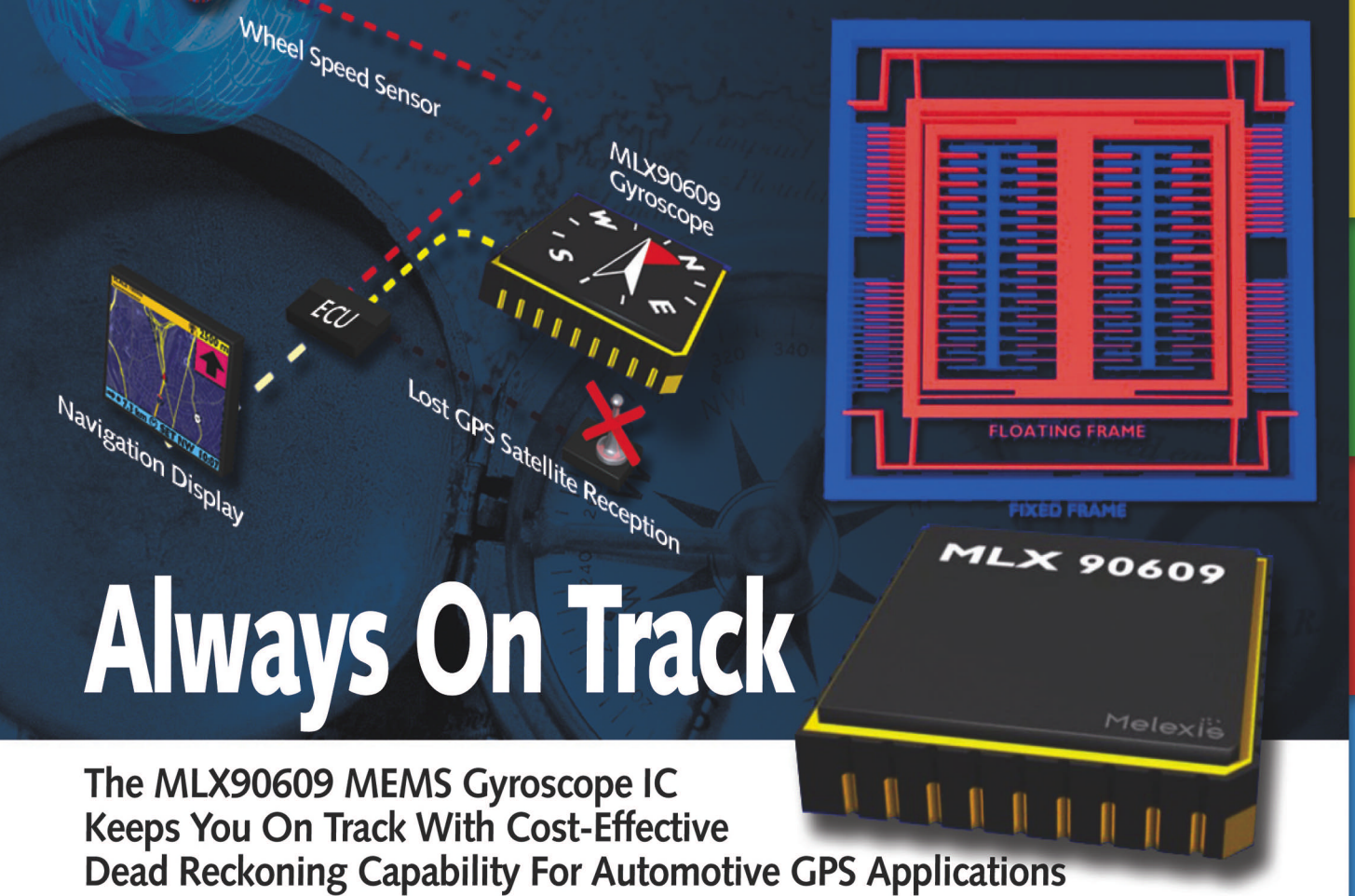
TELECOM GLOBALIZATION

Some uniformity does exist in the requirements of the POTS (plain-old-telephone system), at least in how the equipment works. Regulatory standards that the phone equipment must comply with vary from country to country, however. No one knows this fact better than the designers at Silicon Labs. Many years ago, they set out to design a modem that would comply with every standard in the world. Thus, they created the Isomodem line of chips. The name of one system block of all modems, the DAA (direct-access arrangement), provides a clue to the challenges that designers face. The chips must ultimately interface with the real-world twisted-pair wiring, which can encounter lightning strikes and line-cross events. A line cross occurs when the electric power that is running on the same utility poles as the telephone lines breaks and falls across the phone line. In some regions of the United States, those utility poles carry 440V-ac power, and peak voltage is more than 600V. European lines, on the other hand, directly distribute 240V. Nevertheless, the standards for the line-cross event differ all over the world. In the United States, FCC Part 68 specifies the design limits and testing and requires surge testing at 1500V. In Europe, European standard EN55024 specifies the limits and does testing at 1000V. Real-world conditions are even more demanding: A line-cross event may generate only a few hundred volts on a phone line, but a lightning strike can generate far more voltage, and the rise time of that event will be short. Designers at Silicon Labs have seen field voltages of 4500V.

Jim Judkins, marketing manager at Silicon Laboratories, points out that flexibility is key. "Our Isomodem has to work in 100 countries," he says. "About half of those have requirements similar to FCC Part 68. Other countries seem more interested in providing barriers to entry to their markets rather than a reasonable standard. The Isomodem has 40 registers to tailor its performance for all these disparate markets. We can vary dc termination, ac impedance, ringer impedance, and many other analog parameters." Digital control and supervision of analog functions provide flexibility, just as Summit Microsystems (www.sumicro.com) uses digital control over analog-power functions to achieve flexibility in that realm. Judkins says the company's customers must use the appli-

(continued on pg 108)

You can reach Technical Editor Paul Rako at 1-408-745-1994 and paul.rako@reedbusiness.com.



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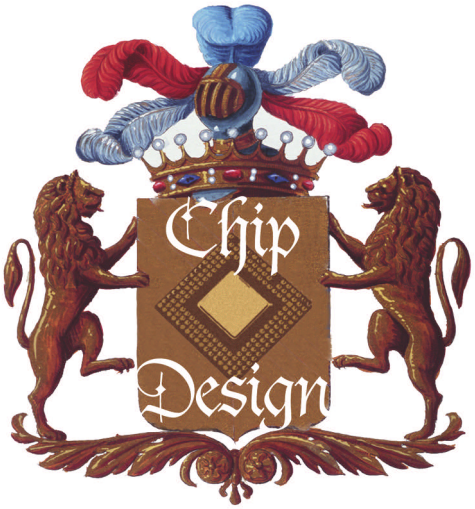


IP plays cautiously in emerging markets

BY MICHAEL SANTARINI, SENIOR EDITOR

As systems and semiconductor companies tap into emerging countries such as China, India, and Russia for low-cost engineering resources, most of the biggest IP (intellectual-property) companies are also doing business in those countries. But doing IP business in emerging countries comes with some risks of piracy and cloning; accordingly, most IP companies have established restrictions on who in emerging countries they will do business with, and some have restrictions on what types of IP they offer to customers in those countries.

ARM, MIPS, Tensilica, and ARC all offer microprocessor IP, and Synopsys is the biggest vendor of utility IP. All are doing business in emerging countries, but if you are tapping into engineering resources in Russia, India, and especially China, for example, you may be surprised to learn that you may have to settle for IP that the vendor has hardened ahead of time, or you may have to go to one of the IP vendor's "trusted" foundries or design houses to have them harden an RTL version of the core for you. Why? IP vendors are terrified at the notion that the RTL version of their code will show up on some Web site and essentially become freeware in countries that don't yet strictly enforce—or in some cases, don't have—solid IP-protection laws. IP has become an essential part of IC designs, and most designs today, especially advanced designs, have tens, hundreds, and—someday soon—thousands of IP blocks (**Figure 1**).

PROTECTING RTL

Traditionally, IP vendors have offered their cores in two formats: soft and hard. A soft core is an RTL-code version of a piece of IP, which the customers synthesize into their design; a hard core has already been synthesized by the IP vendor and is in GDSII (Graphic Data System II) format. Even in the most legally secure countries, IP vendors prefer customers to license a hard version of their IP, because it is relatively difficult to copy and because it prevents customers from fiddling with the code and causing design headaches and royalty-payment delays. But in countries in which the IP laws are questionable, most IP vendors have even tighter restrictions; some don't allow up-and-coming native companies direct access to their RTL.

These circumstances can cause problems, because most designers today would prefer to have the soft version of a core to target their design to a given foundry's low-power process, high-performance process, or higher yield process. Using a hard core means you are stuck with what the IP vendor has implemented, and you can't synthesize the core with the rest of your design to ensure that it tightly weaves into the fabric. It becomes especially problematic as

processes shrink below 65 nm and are subject to process variations that the IP vendor may not have accounted for in hardening the core.

Bruce Beckloff, vice president of investor relations at ARM, notes that over the course of ARM's existence, the customer preference for soft cores over hard cores has swung back and forth many times. Today, ARM offers customers IP in three formats: a soft version in RTL source code, a quasisoft core that is partly RTL with a good percentage that is hardened, and hard cores in GDSII format.

Beckloff admits that over the last few years, with foundries offering multiple flavors of a given process, customers have strongly preferred the flexibility of soft cores. ARM, he says, is seeing that preference change with its newest microprocessor architecture, the Cortex-A8. "If you look back to 1995, we started offering a quasisynthesizable ARM7, but people said it was too hard to synthesize and asked for hard cores," says Beckloff. In 2002, he notes, "The pendulum swung the other way, and folks wanted synthesizable cores. Now, [ARM] offers the Cortex-A8, which is a quasisynthesizable core with a few hard bits, and that is more where the fashion is right now. People are fine with us doing the hardening, because we know the core, and we can do it in a better way than other guys. But the big licensees are always going to want the RTL." However, he warns, "There is a cost that comes with that flexibility."

MIPS, Tensilica, ARC, and Synopsys say that all things being equal, customers overwhelmingly would like at least access to the RTL. However, in the ever-growing global market, that access depends on many variables, including the size of the company, its status in the world market, and, most recently, the location of the design group.

"If we lost our RTL, it would be a major issue," says Jack Browne, vice president of marketing at MIPS. "We've done 200 contracts with 118 customers. About 50 are shipping silicon, and they have about 850 different chips. So there are a lot of chips out there." Browne contends that because MIPS has "pretty good" silicon, it would not be beneficial to the company if its RTL got out. "We'd have good market share," he notes, "but our financials wouldn't be so good. We want our customers to treat our cores like they treat their own IP."

GEOGRAPHIC RESTRICTIONS?

A big question in the IP industry is what to do in regions of the world where other people's IP does not receive the proper respect. "China, India, and Russia are a few of many examples of countries that don't yet fully respect others' IP," says Browne. "We, as do many, believe as indigenous companies in these countries build their own IP, they'll want to protect it, and the overall practices will change. In the future, life will be better, but today, how do we deal with it?"

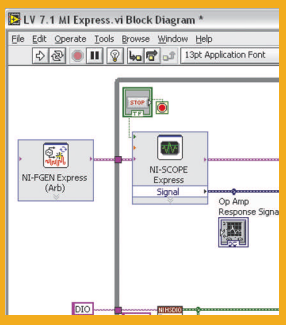
MIPS deals with it by not providing RTL versions of its cores to most customers in emerging countries. Browne says that MIPS requires customers in emerging countries to work directly with "MIPS trusted partners"—foundries and third-party design-services companies. According to Browne, when customers from emerging countries approach MIPS, the company refers them to one of its trusted design partners, such as Cadence Design Systems, Synopsys, Wipro, OpenSilicon, or, in China, IPCore. The customer builds most of the design and leaves a hole in it for the core. He then sends the design to a MIPS partner that is certified to use

SYNOPSYS EVALUATES CUSTOMERS IN CHINA

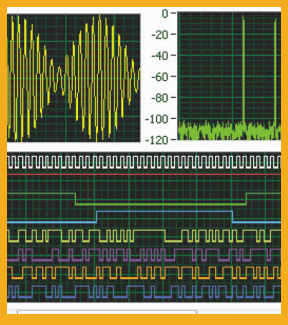
Synopsys has been offering IP (intellectual property) in China for five years, and in that time, the company's vice president of marketing for the IP group, Guri Stark, has developed a philosophy for licensing IP in China. Stark claims that there are currently four types of IP customers in China. The first are Western companies that have their headquarters in the Western world but with operations in China. The second are large Chinese companies that have operations in China but have aspirations to sell outside China. The third type of IP customers are the more-than-500 start-up design shops in China that are doing low-level designs targeting the high-volume but cost-conscious market in China. The fourth type of customer is a slice of those 500 companies that have had some success selling to the high-volume but cost-conscious market in China and now have venture capitalists lining up to give them money. "If it is a Western-based company, I don't have any problem selling them any type of IP, if the contract is signed at their headquarters in the Western world," says Stark.

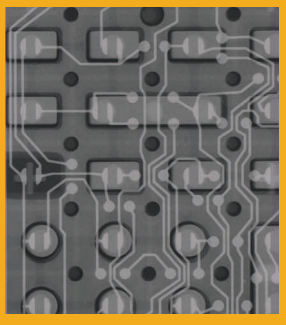
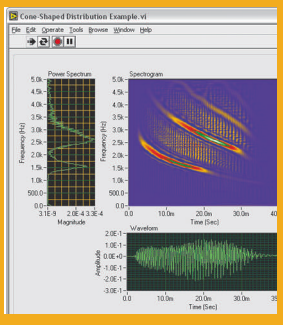
Stark says he will also sell IP with no restrictions to large Chinese companies that aspire to sell outside China, because most of those companies have established IP policies in place that they can prove. He notes that those companies will have policies that don't allow cameras in their buildings and don't issue laptops with USB or other external drives (a bit ironic, because Synopsys sells USB).

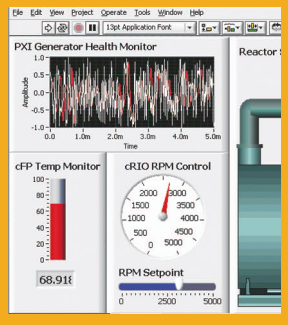
Where Synopsys starts to have a problem with licensing is with the third and fourth types of companies. "I have problems selling them IP," says Stark. "I'd love to sell to them, but we have to be extremely careful." Of the companies that have seen success, Stark says, many of them have lots of money and are starting to implement some forms of IP protection. "Selectively, after you visit them and look at their site, and after substantial evaluation, you can sell them IP." Stark notes that Western-educated executives–who have lived and worked in the Western world but now have returned to China–are starting to run many of these start-ups. "They understand and respect the importance of IP," he says.

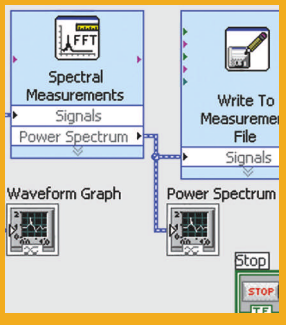





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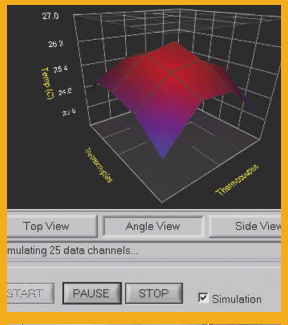



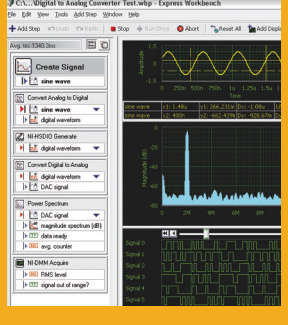

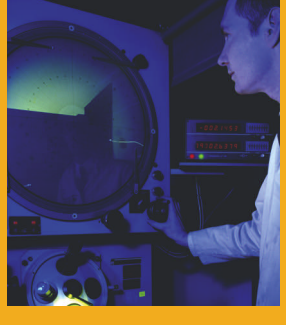
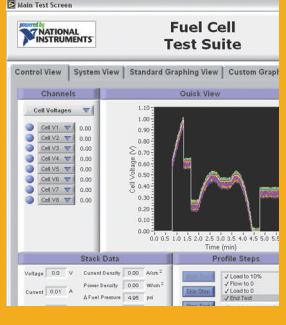

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the RTL. That partner then synthesizes the core into that design and then sends the GDSII back to the customer. The customer never sees the RTL.

Two years ago, MIPS established its own hardening group in China. In 18 months, this group has hardened four cores. MIPS also offers hard cores directly to customers in emerging areas. "We do a process-specific, configuration-specific design delivered in GDSII with a bus functional model, a Verilog model for timing, and MIPS Sim instruction-set simulator and aspect-ratio pinout," says Browne.

But using the trusted-partner method also provides MIPS with indemnity, should the design violate other patents or be defective. Although it does restrict native customers in some geographies, such as China, Browne says MIPS doesn't have licensing restrictions on Western companies that have design groups in China, because they police themselves. MIPS has also instituted a program to ensure consumers that they are getting a legitimately licensed core

ENABLING A GOLDEN OPPORTUNITY IN CHINA

By Bill Martin, General Manager, Mentor Graphics IP Division

Protection and piracy of IP (intellectual property) have caused many companies based outside Asia to avoid business with companies in the Pacific Rim. From electronics and semiconductor IP to film and even music, numerous technical and business articles have tackled this subject–reinforcing the fact that many companies fear that their products will be pirated throughout the Pacific Rim. Compound that fact with the global shifts toward outsourcing and sending business off-shore, and it becomes obvious why there are enormous concerns with IP throughout this region.

Companies in the United States, Europe, and Japan have seen the resurgence of third-party IP to meet today's consumer demand for leading-edge technologies. Most IP vendors have avoided the Pacific Rim, because any form of IP (digital, analog, or software) protection can be broken or re-engineered, increasing the risk of IP piracy. The lack of readily available IP forces companies in the Pacific Rim into different behaviors. They can either fully develop the IP in-house or obtain the IP through friends or acquaintances that have access. Most consider the latter approach to be piracy, and the former increases the possibility of an unsuccessful or delayed product launch.

With the Pacific Rim, and particularly China, which is poised to be the "Silicon Valley of the East" and a potential gold mine for business, does it make sense to avoid the opportunities this region holds? Although some of China's business and cultural practices differ from those practices in the United States and Europe, IP vendors and IP consumers must develop trust with each other.

As the industry's second largest standards-based-IP provider in EDA, Mentor Graphics decided to embrace China. Building trust is critical to tearing down the barriers between nations and is achievable through openly and honestly sharing information with an explicit understanding of what the relationship hopes to accomplish. Mentor has recently established an exciting and dynamic business relationship in China with one of the world's leading semiconductor foundries, but this relationship didn't happen overnight. Instead, through Mentor's regional alliances in the Pacific Rim and face-to-face communications at all levels of management, from the technical staff to executives, Mentor began to build a connection with this company.

Having discussions of mutual business goals and objectives, understanding and respecting cultural differences, and realizing mutual risks and rewards were keys to establishing a lasting relationship.

Not surprisingly, there were some roadblocks in these discussions, such as those regarding product-development time lines, prices, and support. These issues came up immediately, and Mentor and the semiconductor foundry openly discussed them. Addressing key issues with key decision makers was paramount to the success of this endeavor. When conflicts and technology glitches occurred, the two companies did not hold firm to what they had already established; instead, they openly discussed and reassessed their mission, their value to one another, and the desire to succeed.

Over the past year, Mentor has conducted numerous discussions and meetings with its Chinese partners. It's an incremental process, to be sure. But the dividends are well worth the investment. As a result, Mentor has developed new business models and opened up new distribution channels with its new Chinese partners, and Mentor plans to see profitability over the coming years. Likewise, Mentor's partners in China want to see the issues of IP piracy improve, and they are now seeing increased levels of confidence with IP protection and IP-business development in Asia.

IP piracy is indeed a huge problem in the Pacific Rim. But if Mentor's experience is any indication of the future, the company is now at the forefront of establishing a global infrastructure of truly historical proportions.

AUTHOR'S BIOGRAPHY

Bill Martin is the general manager of Mentor Graphics' Intellectual Property division, the industry's second largest standards-based IP provider. He has more than 25 years of experience in consulting, product design, and project management and holds five patents. Martin joined Mentor in 2000 as US director of Mentor Consulting and was promoted to vice president of Mentor Consulting. He had previously worked for Synopsys and VLSI Technology. Martin holds an MBA in Marketing/Finance from the University of Texas at Dallas, and a BS in Computer Engineering from the University of Illinois, Urbana.

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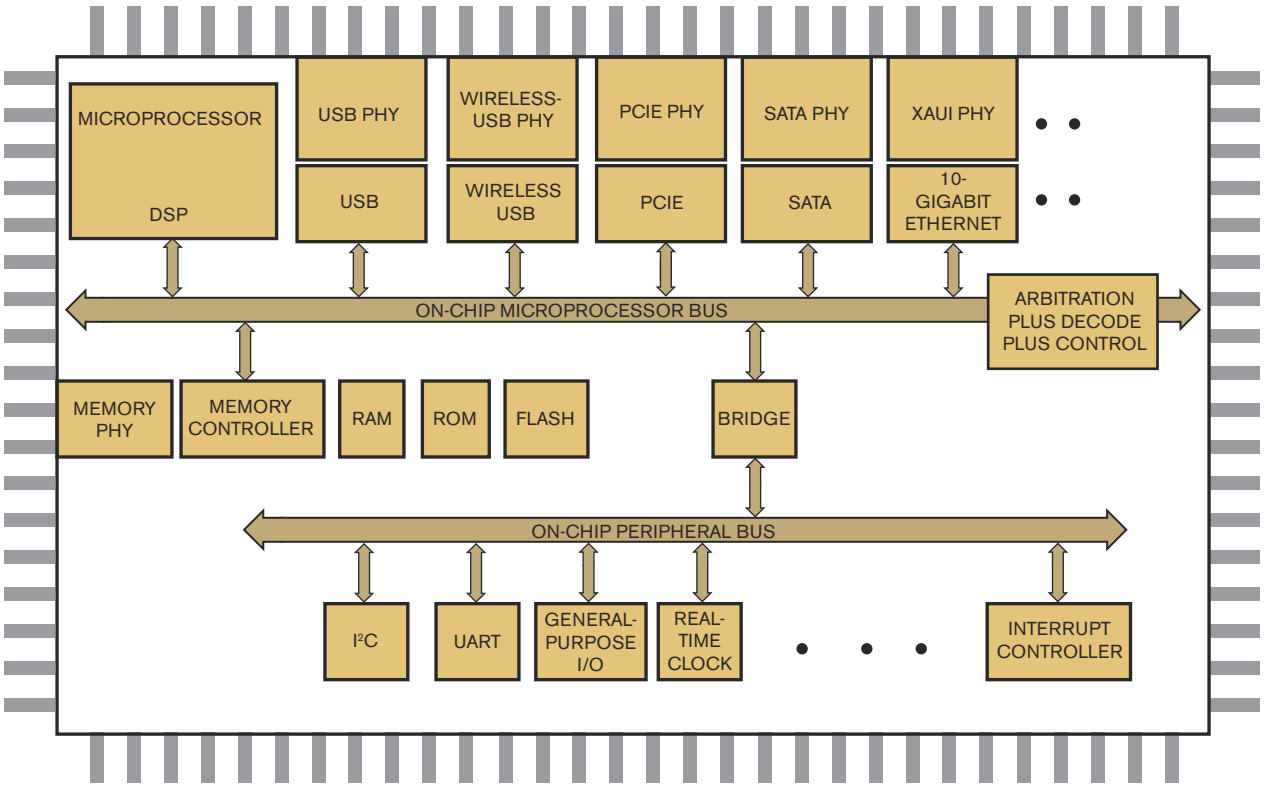

Figure1 IP has become essential to IC design. It is hard to find an advanced digital design today that does not contain multiple IP blocks.

from MIPS. The company will add "MIPS verified" to the device and product literature to ensure its verification. But, of course, other companies can copy the words "MIPS verified," too.

ARM is by far the oldest and largest microprocessor-core vendor worldwide and has been doing business in China for 10 years, the longest of the large IP vendors. During that time, ARM has established design and sales offices in the countries that Beckloff says offer one level of deterrent from IP theft. The idea is that people are less likely to steal from a friend.

Beckloff says that ARM has no geographic-specific restrictions when it comes to what format of a core it will offer customers but that the company favors offering the hard version of its core to start-ups or companies in China or other countries that don't yet have a global presence. He notes that ARM's single-use license is typically the best option for start-ups in China and elsewhere, because it has a lower up-front cost, allowing companies lacking up-front funds to quickly get a design to market. Hard cores, says Beckloff and many others, are typically more reliable, because the vendor has likely verified and perhaps even manufactured the core, potentially meaning less engineering and verification for the customer. But those single-use hard-core licenses also typically require customers to pay much higher royalties than they would if they paid the higher up-front fee for a traditional four- to seven-year design engagement, which often has lower per-chip royalties.

Customers in Asia can get single-use licenses through ARM's foundry program. "These licenses allow you to take a single design to our core," says Beckloff. "You get a black box of the core. You input signals, and you get an answer out, so you don't have the internals of the design." Therefore, says Beckloff, it is a more secure way of providing the IP. He continues, "Certain regions find that approach more valuable. So, in regions like Taiwan, Israel, and China, where most of the companies making the decisions are actually the start-ups creating the new industry, more times than not they will be using a single-use design license." Beckloff believes this situation stems partly from security concerns and partly from licensing preference. "With certain companies like start-ups, you may limit the flexibility you give. In turn, you may get a product with a more cost-efficient price."

Like MIPS, Tensilica also has some geographic restrictions. Tensilica offers preconfigured cores, like ARM and MIPS do, but it also offers configurable cores. Its Diamond preconfigured lineup is available in hard, encrypted, and soft formats. "The hard cores we do with partners like Global Unichip (TSMC) in Taiwan and SMIC for the China market," says Steve Roddy, vice president of marketing for Tensilica. "We also offer an encrypted RTL core, which puts up additional barriers for someone who might want to misappropriate our IP, and we offer pure source RTL."

Tensilica is also protective of most of its RTL. "We'll offer RTL cores in the

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right circumstances to people all over the world," says Roddy, noting that companies are more likely to offer the hard cores and encrypted flows in geographies where people have more concerns about legal systems. "China is the one most people are concerned about, because they don't have the precedent court cases that allow you to work things out correctly." Roddy points out that companies that are going to sell products to markets outside China are less worrisome, because reputation matters.

In addition to offering preconfigured microprocessor IP, Tensilica's claim to fame has been its Xtensa line of configurable cores. Interestingly, Tensilica is less worried about piracy of Xtensa processors than of Diamond processors, even though after users have customized their processor using Xtensa, they essentially get RTL code. Roddy says that users configure those cores to suit their product lines, so, in a way, they are motivated to ensure that their version of the core doesn't get into competitors' hands. "As long as the customer has his skin in the game, he's going to keep an eye on it," says Roddy. "If it is just something you bought from an outside supplier and if it leaks out, it doesn't hurt you personally. The degree of care you are going to put into security measures is naturally going to be less, because 'What do you care?' We have unique advantages. Companies offering just preconfigured cores don't have that flexibility."

Tensilica's competitor in the configurable-microprocessor market, ARC International, echoes this sentiment. But where other vendors are more cautious about the location of customers, ARC is open to all comers in all geographies. "When we go into a region, we look at the product requirements within that region rather than what we do or do not want to provide there," says Derek Meyer, ARC's senior vice president of SOC (system-on-chip) sales and marketing. "When we moved into Taiwan about 18 months ago, we looked at what the market requirements were and immediately served the market there based on those requirements. As we've now moved into China, we've done the same thing."

ARC in September introduced its first market-specific product for the Chinese market, ARC Player, an entry-level multimedia-IP block. "It targets a growing market in China," says Meyer. "Some companies will treat others as second-class customers and restrict the availability of products—we don't do that." ARC builds products such as ARC Players for particular markets, he continues, but such products are synthesizable with a media codec. The company, says Meyers, licenses the IP core to all regions simply as a synthesizable product with a media codec.

ARC offers the Architect tool, which Meyer says serves as a safe-delivery mechanism. "It allows us to send our source encrypted," says Meyer. "When customers perform a configuration, it decrypts and hands them the RTL they specified. But at the end of the day, it is RTL unique to them."

If customers don't want to engage with ARC in a traditional IP-licensing model that has an engagement fee and manufacturing royalties, the company also offers its IP in an annual-subscription format, which Meyer says is basically a "smorgasbord license" that allows customers to implement the core in an unlimited number of designs and manufacture an unlimited number of ICs free of royalties. "Obviously, it is a higher rate, but we do have customers under that license today," says Meyer, noting that the license is usually more attractive to large companies.

Meyer says Asia represents about 30% of ARC's revenue today, but that figure was practically zero three years ago. He attributes much of that growth to ARC's lack of geographic restrictions.

Synopsys, which is the largest supplier of utility cores (just about everything else in an IC, in addition to some microprocessors and microcontrollers), is a bit more cautious about offering its IP to customers in emerging countries. MIPS and Tensilica have now been in China for two years, and ARC arrived there only recently, but Synopsys has been in China for five years.

A few years ago, Synopsys tried the trusted-design-services-partner method that MIPS now employs for handing off its RTL to China-based companies. But it didn't work for Synopsys, says Guri Stark, vice president of marketing in the IP and systems-solutions group. "A plan that depends on a trusted vendor in China may be difficult to scale, unless the vendor has the size and ability to sell to the top segments."

Stark says that in China, a government-sponsored effort is currently underway to come up with neutral design sites that allow IP companies and vendors to work together on designs, and nothing but GDSII leaves the site. Stark maintains that with China's having such huge potential as a growth market, the effort warrants further investigation. Until the program shows solid proof that it works, Synopsys will enforce some restrictions on the cores and formats it offers to vendors in China and other emerging countries (see **sidebar** "Synopsys evaluates customers in China").

"We offer mixed-signal PHY [physical-layer] cores, but those are inherently in GDSII format, so I'm not so worried about those," says Stark. But he's cautious about offering USB cores in RTL format, because they are easy to copy and harder to track. Indeed, much of the IP that Synopsys offers has an inherently shorter shelf life than what microprocessor-IP vendors offer. As time moves on and much of its utility IP becomes simply a commodity, Synopsys can bundle the commodity IP as a set of macro library functions with its EDA software—traditionally its main business.

Because of this situation, Synopsys doesn't monitor royalties as diligently as do the microprocessor-core vendors, who draw most of their revenue (and livelihood) from royalties. Because their existence depends on royalties, the big IP vendors often conduct expensive audits of customer IC production. But monitoring IC production and royalties

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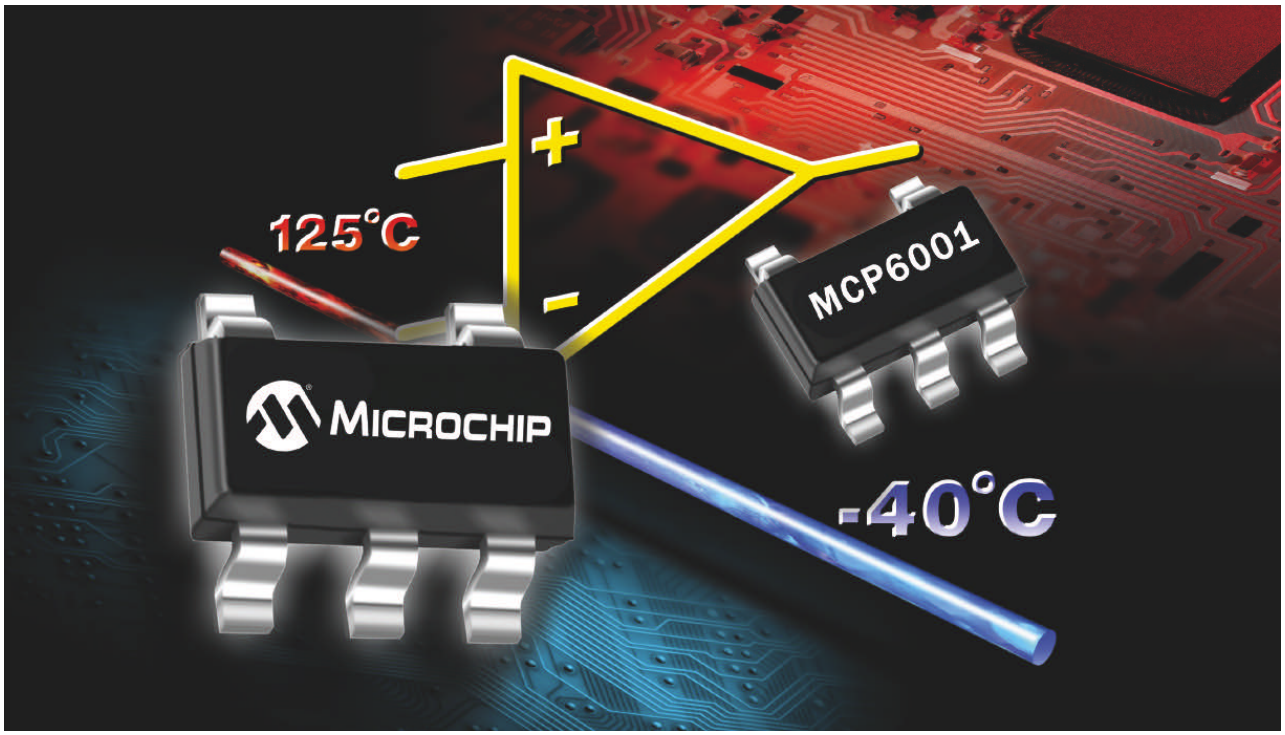

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MCP6241/2/4	550 kHz	50	5.0	45	1.8 – 5.5
MCP6001/2/4	1 MHz	140	4.5	28	1.8 – 5.5
MCP6271/2/3/4/5	2 MHz	170	3.0	20	2.0 – 5.5
MCP6281/2/3/4/5	5 MHz	445	3.0	16	2.2 – 5.5
MCP6291/2/3/4/5	10 MHz	1100	3.0	8.7*	2.4 – 5.5
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can also be more troublesome in emerging countries in the expanding global design environment.

ROYALTIES AND PROTECTION

Without exception, the large IP vendors derive the bulk of their revenue from royalties, which allow an IP company to get a percentage of every chip that a customer produces for as long as it produces it. But, in some emerging countries, inventory tracking can be questionable. Off-the-books production is common in some emerging countries. In this scenario, a manufacturer produces a number of products for the customer but then secretly manufactures an excess that it does not record in the books. Often, the manufacturer sells the products on the black market to serve as pure profit (as they require no royalty).

But the IP vendors say that as far as they know, off-the-books production isn't a problem today in the IP—let alone the IC—industry, and they don't expect it to become a problem in the future, given that the chips run through foundries that have a huge stake in keeping track of units and staying legitimate in the eyes of the world market. In the end, however, most IP vendors admit that there isn't yet a foolproof way to track IP and stop off-the-books production from happening if it did occur. "Royalties are completely based on trust," says Stark.

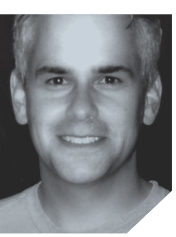
Still, IP vendors have a habit of checking, and most IP companies have traditionally employed two control mechanisms for monitoring manufacturing royalties. The first is watermarking, in which manufacturers place a distinctive symbol or serial number on each layout. Most IP vendors realize that cracking into a chip and trying to find the watermark under the layers is cost-prohibitive. But there are companies that have come up with more sophisticated production-monitoring systems, such as one that Certicom offers that can read watermarks using a testing device. Inserting those systems into an IC-production run requires buy in and proper use from the foundries.

The second control mechanism that IP vendors use to track royalties is auditing. All of the big IP vendors write into their contracts that they reserve the right to audit customer books. This stipulation allows them to double-check customer chip production and ensure that the customers are paying their per-chip royalty. But, again, it is costly to hire an accounting company to conduct the audit, so most companies hire accountants for only their largest customers. MIPS, for example, audits most companies every two years, doing approximately five audits a quarter. "We tend to visit people that are shipping a lot of product," says MIPS' Browne. "Sometimes, they overpaid us; sometimes, they owe us a lot of money. But by and large, the audits are coming back, and things are within a reasonable level; people are pretty honest."

ARM's Beckloff says that ARM hasn't run into big auditing issues either, but, as the IP industry matures and expands, such issues will likely become more difficult to manage. "Keeping track of all the designs, especially when it has gotten to the scale it has gotten to at this point, is actually very difficult," he says.

Overall, emerging countries, such as China, India, and Russia, pose great opportunities for companies that want to tap into the low-cost-design pool and sell products to billions of customers (see **sidebar** "Enabling a golden opportunity in China"). But if you are a start-up designing a chip in China or have contracted with a chip-design-services company there, don't be surprised if IP vendors are a bit more cautious about licensing their RTL and if they push you to license either a hard version of their core or have you work with one of their trusted third parties or foundries. None of the IP vendors say that they are currently in a piracy dispute with another company. It might be that their precautions are working, that they are getting ripped off and don't know about it, or simply that IP-cloning and -piracy problems aren't happening at all. It may be too early to tell, because most of the IP vendors have only recently entered the new markets. EDN

You can reach Senior Editor Michael Santarini at 1-408-345-4424 and michael.santarini@reedbusiness.com.



ANALOG *(continued from pg 97)*

cation staff to ensure that they are properly designing the part into the target system. In addition to the applications group, he points out, the company also has a compliance-engineering group, which ensures that customers understand all the regulatory requirements that countries place on the product.

The ability to break a large project into many pieces that engineers worldwide can work on is the driving force behind object-oriented design, as well as digital design. Designers cannot partition analog designs in this manner. They must be privy to the needs and architecture of the entire system. All analog parameters interact, meaning that they more severely feel the effects of the real-world requirements that globalization presents. Fortunately, innovative analog companies are meeting these challenges. The challenge of design for a global marketplace is just another requirement for analog designers, along with cost, thermal effects, size, speed, and time to market. With the advent of new, exciting space programs, the opportunities for analog will be out of this world. EDN

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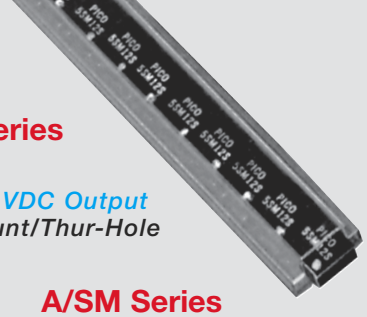

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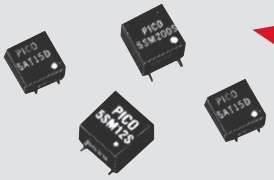

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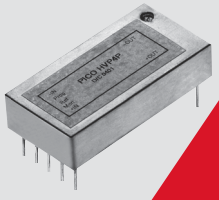

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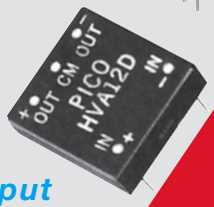

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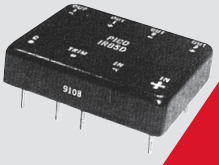

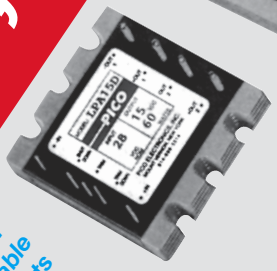

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Fixed-point-IIR-filter challenges

IIR FILTERS CAN MEET HIGHLY SELECTIVE MAGNITUDE-FREQUENCY-RESPONSE SPECIFICATIONS WITH A LOW-ORDER APPROACH. AS SUCH, AN IIR IS OFTEN THE TECHNOLOGY OF CHOICE IN REALIZING FREQUENCY-SELECTIVE TONE DETECTORS, NARROWBAND SPECTRAL FILTERS, NOISE REJECTERS, AND DIGITAL CONTROLLERS. THEIR DESIGN, HOWEVER, ENTAILS SOME UNIQUE CHALLENGES.

The historic role of IIR (infinite-impulse-response)-filter-design software is to translate a set of frequency-domain design specifications into a transfer function that is based on recognized IIR-filter models. You can use any of dozens of commercially available software packages to synthesize a transfer function from a set of user specifications. The SPT (signal-processing toolbox) and FDATool (filter-design and -analysis tool) in The Mathworks' (www.mathworks.com) Matlab, for example, contain many of the objects you need to synthesize an IIR-transfer function. These functions include Matlab's Butterworth, Chebyshev I, Chebyshev II, elliptic, Burg-AR (autoregressive), covariance-AR, and Yule-Walker-AR functions. You use the first four deterministic filter classes to synthesize a classic fixed-coefficient filter based on user-specified passband-critical frequencies and maximum attenuation and stopband-critical frequencies and minimum attenuation. The last three design methods synthesize AR, fixed-coefficient, feedback-only IIR filters in terms of measured or desired input/output spectral responses.

The choice of which filter model to use is generally not the issue. Often, the designer specifies or selects the IIR type from a restricted list. For performance and cost reasons, designers generally prefer fixed-point approaches over floating-point instantiations. Unfortunately, fixed-point designs are highly susceptible to a range of degrading finite-word-length effects,

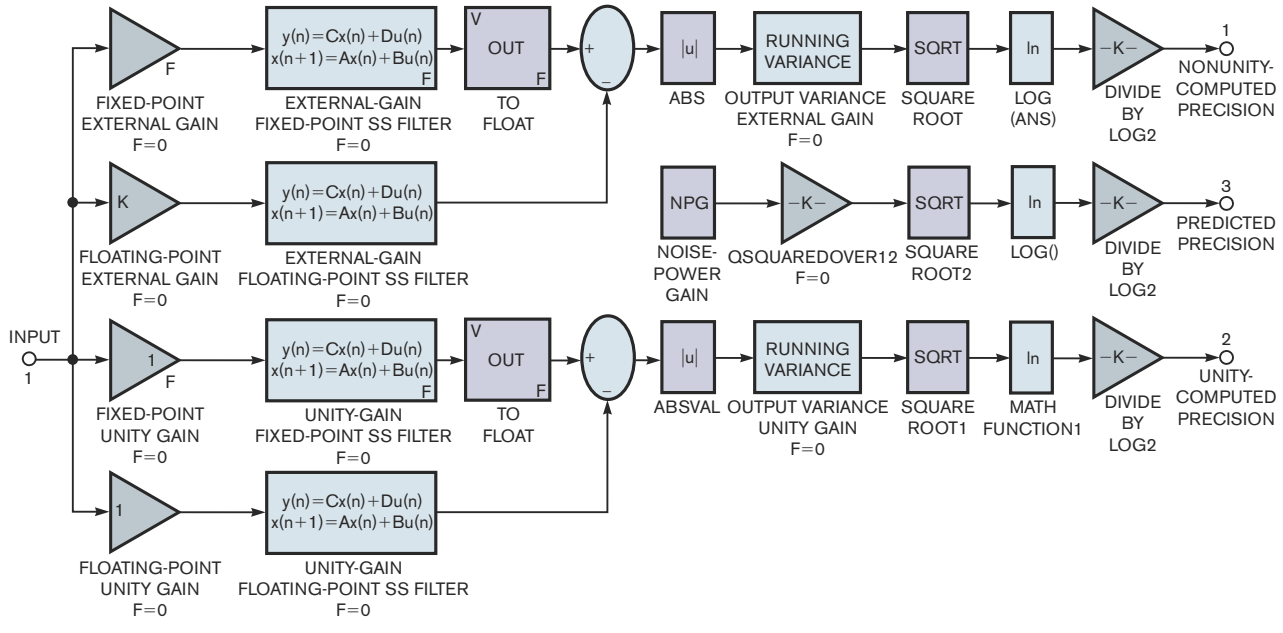


Figure 1 A Simulink simulator tests the behavior of a 16-bit filter for fractional precisions ranging from Fϵ[0,15].

in some cases rendering a design unusable. As a result, you must take extreme care to ensure that the final outcome meets the target design requirements.

FINITE-WORD-LENGTH EFFECTS

The goal of a fixed-point IIR-filter design is to maximize filter performance and minimize finite-word-length effects, which include register overflow and arithmetic-round-off errors. The more egregious error is register overflow, which occurs whenever a filter's dynamic-range requirements exceed the dynamic-range limitations of a fixed-point register. Arithmetic-round-off errors result from imprecise arithmetic, which in turn reduces precision. Register overflow can cause a system to behave in an unpredictable, nonlinear manner, producing potentially large runtime errors. In the absence of register overflow, a system behaves linearly but possibly with degraded precision due to the accumulation of various arithmetic errors accumulating within a filter. A filter-design engineer should be able to quantify and control the effects of arithmetic errors to ensure that the final outcome meets some minimum precision requirement. This process begins with making design choices. Although the filter type may be non-negotiable, the choice of architecture normally is negotiable. The choice of architecture is a critical factor in controlling finite-word-length effects.

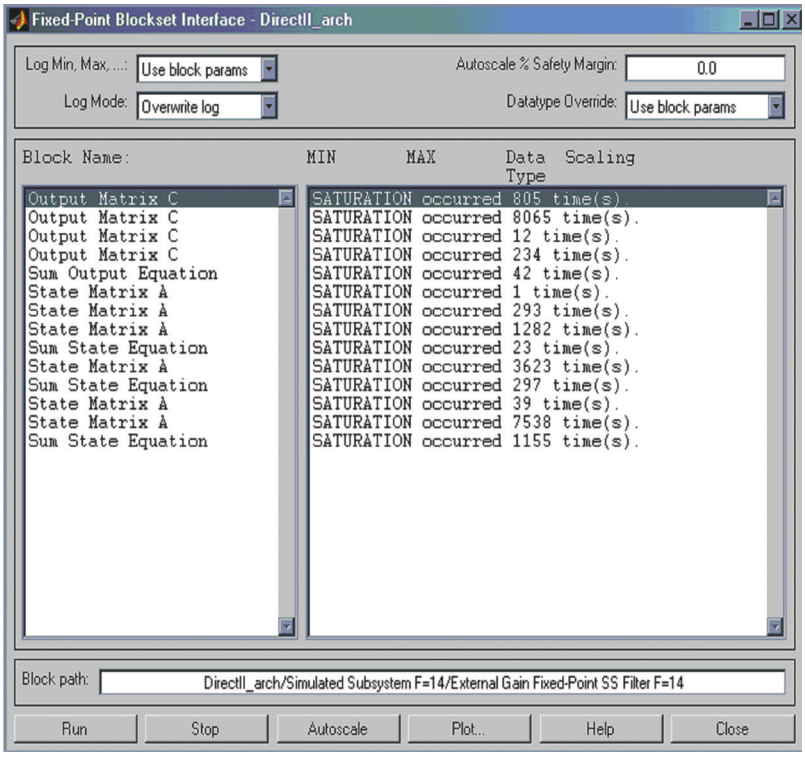


Figure 2 When the simulation is complete, you can use the fixed-point GUI to examine runtime-saturation effects.

REGISTER OVERFLOW

The most serious finite-word-length effect is register overflow. Register overflow introduces large nonlinear distortions into a system's output, often rendering a filter useless. A filter designer must eliminate or control the effects of runtime register overflow. Some standard techniques are available to mitigate this problem. One effective means of controlling fixed-point-overflow errors is to perform all arithmetic using a two's complement arithmetic unit. Two's complement possesses the important modulo(2^n) property that ensures that the sum of a string of two's complement numbers is a valid two's complement outcome, ensuring that the accumulator does not overflow. Alternatively, designers can use a saturating-arithmetic approach. A saturating-arithmetic unit "clamps" a register's contents at the register's extreme values if overflow occurs. Even with saturating arithmetic, the effect of register overflow creates serious errors.

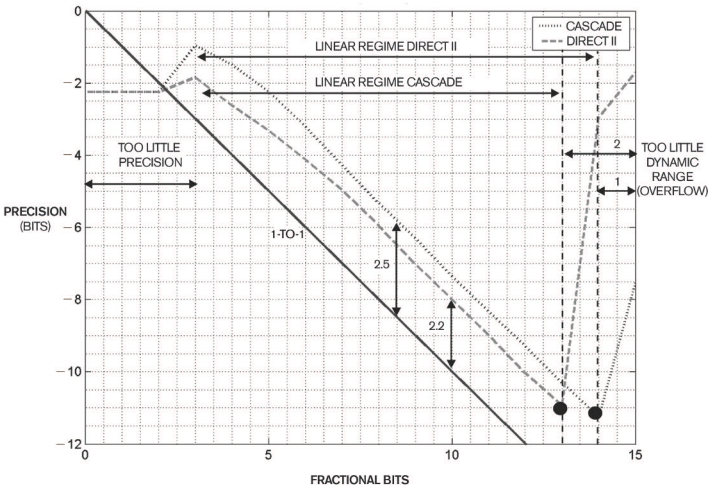


Figure 3 With the simulated output, you can partition the results.

Scaling the input to a lower level can eliminate register-overflow conditions. Experimentally determining the required scale factor can be a tenuous approach. Furthermore, the test inputs may not represent an input-worst-case event and therefore may underestimate scaling needs. Scaling reduces the precision of the input, which in turn reduces output precision. Another means of eliminating runtime overflow is to use extended-precision arithmetic and registers. Extended-

(continued on pg 120)

IIR-FILTER ARCHITECTURES

You define the physical implementation of a digital filter in terms of its architecture. "Architecture" refers to how a designer builds a filter using primitive building-block elements, such as shift registers, memory, multipliers, and adders. Many DSP-system engineers are generally aware of only one or two possible filter architectures. However, many architectural choices exist, each carrying relative advantages and disadvantages. Some architectural choices are application-specific, and others have general-purpose implications. Some provide better control of finite-word-length effects, and others emphasize reduced complexity and increased speed. The more common architectures are Direct I, Direct II, cascade, parallel, normal cascade, normal parallel, lattice/ladder, wave, and biquadratic.

The two most popular architectural choices are Direct II and cascade. However, all can implement a given transfer function, H(z). If you build an IIR (infinite-impulse-response) filter using floating-point arithmetic, then all architectures would have identical input/output behavior. This behavior is not the case when you implement designs using fixed-point arithmetic. Fixed-point arithmetic gives rise to finite-word-length effects that can degrade a filter's performance. The choice of architecture, in turn, strongly influences the severity of these errors. It is therefore essential that fixed-point-IIR-filter developers know how to exercise control over the design environment and minimize the impact of these errors on the outcome.

An IIR filter's transfer function, H(z), which you produce using The Mathworks' Matlab or another commercial software tool, quantifies only an IIR filter's input/output behavior. A transfer function, unfortunately, does not quantify the filter's internal workings in which errors emerge and accumulate. The filter's internal structure, or architecture, includes state variables. You use the state-variable model to audit the information entering, exiting, and residing within a digital filter. Equation A illustrates a state-variable model of a single-input, single-output, Nth-order IIR (Figure A). The state-model is $x[k+1]=Ax[k+1]=x[k]+bu[k]$, and the output model is $[yk]=c^T x[k]+du[k]$, where x[k] is the N-dimension state vector of state variables, u[k] is the input, and y[k] is the output. The other elements of the state-variable model are an N×N feedback matrix A, a 1×N input vector b, an N×1 output vector c, and a scalar-direct input/output-path gain d. The filter's N registers store x[k] and x[k+1] on the next clock cycle. Because state-variable models model the internal behavior of digital filters and this information is critical in managing register overflow, understanding the relationship between the state model and a given architecture is important.

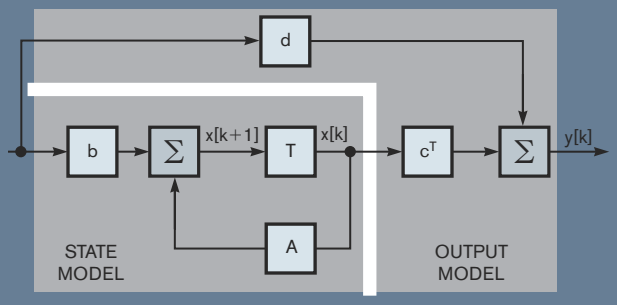


Figure A Understanding the relationship between the state model and a given architecture is important.

The Direct II architecture is a common IIR form. It is based on interpreting an Nth-order IIR transfer function, H(z), as the following equation shows:

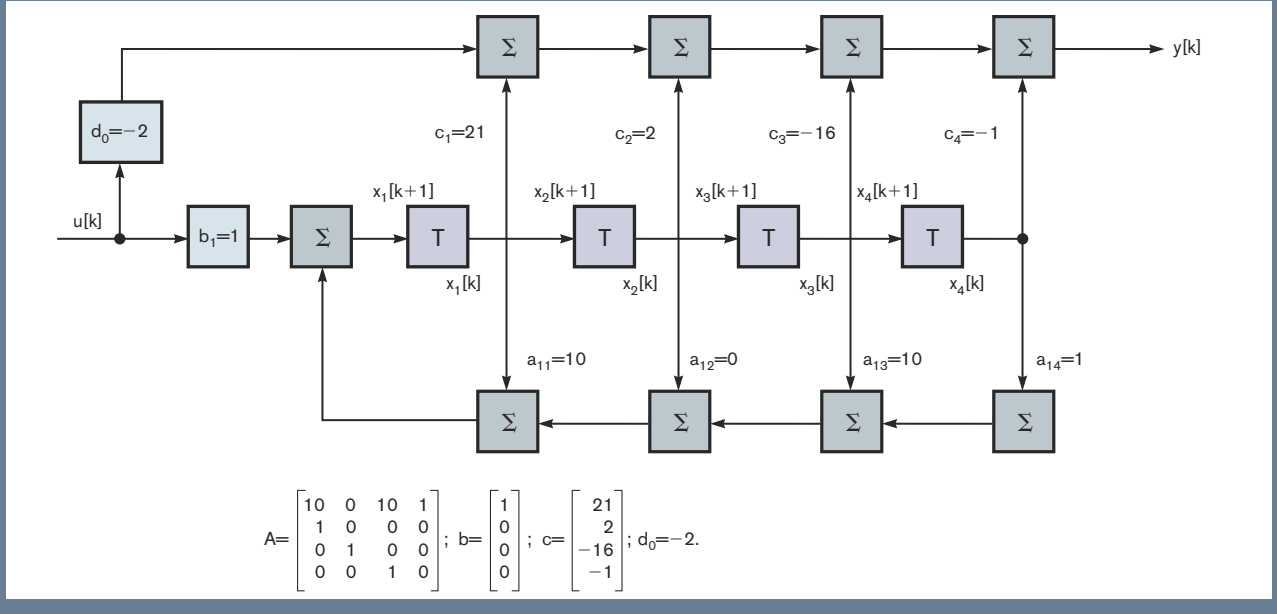


Figure B This Direct II state four-tuple S=[A,b,c,d] induces this architecture.

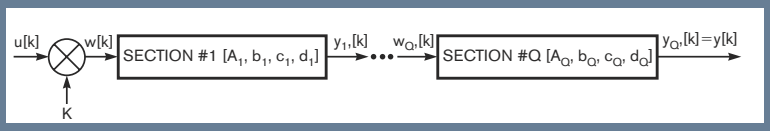


Figure C You use the basic cascade architecture to implement a transfer function.

$$H(z)=K\frac{N(z)}{D(z)}=\frac{b_0+b_1z^{-1}+\cdots b_Nz^{-N}}{a_0+a_1z^{-1}+\cdots a_Nz^{-N}}$$
$$=K\left(\frac{b_0}{a_0}+\frac{(b_1-b_0a_1/a_0)z^{-1}+\cdots+(b_N-b_0a_N/a_0)z^{-N}}{a_0+a_1z^{-1}+\cdots+a_Nz^{-N}}\right)$$
$$=K\left(\frac{b_0}{a_0}+\frac{c_1z^{-1}+\cdots+c_Nz^{-N}}{a_0+a_1z^{-1}+\cdots+a_Nz^{-N}}\right)$$
$$=K\left(d_0+C(z)\left(\frac{1}{D(z)}\right)\right). \quad \textbf{(A)}$$

The following equation yields the Direct II state-variable four-tuple (A, b, c, d):

$$A=\begin{bmatrix}-a_1 & \cdots & -a_{N-2} & -a_{N-1} & -a_N\\ 1 & \cdots & 0 & 0 & 0\\ \vdots & \ddots & \vdots & \vdots & \vdots\\ 0 & \cdots & 1 & 0 & 0\\ 0 & \cdots & 0 & 1 & 0\end{bmatrix};\ b=\begin{bmatrix}1\\0\\\cdots\\0\\0\end{bmatrix}. \quad \textbf{(B)}$$

The (i,j) element of A defines the path gain between state $x_j[k]$ and $x_i[k+1]$, b_i is the path gain between the input and $x_i[k+1]$, c_i is the path gain between $x_i[k]$ and the output, and d_0 is the gain of the direct input/output path. One caveat you should know about is that Matlab state-variable programs make state assignments in a reverse order to what you generally find in signal-processing literature and textbooks.

You can convert the transfer function H(z) into a Direct II form using the Matlab functions TF2SS or ZP2SS. The function TF2SS converts a transfer function, H(z)=KN(z)/D(z), into a Direct II state form using the syntax [A,B,C,D]=TF2SS(NUM,DEN). Similarly, the function ZP2SS converts transfer function H(z) having zeros (Z), poles (P), and input-scale factor (K), into a Direct II state form using the syntax [A,B,C,D]=ZP2SS(Z,P,K).

Consider the fourth-order transfer function H(z):

$$H(z)=\frac{-2+z^{-1}+2z^{-2}+4z^{-3}+z^{-4}}{1+10z^{-1}+0z^{-2}-10z^{-3}-z^{-4}}$$
$$=-2+\frac{21z^{-1}+2z^{-2}-16z^{-3}-z^{-4}}{1+10z^{-1}+0z^{-2}-10z^{-3}-z^{-4}}, \quad \textbf{(C)}$$

which you factor using Equation A. From this factorization, you can construct a database for a Direct II filter. Specifically, [A,B,C,D]=tf2ss([−2 1 2 4 1],[1 10 0 −10 −1]).

A=−10 0 10 1 1 0 0 0 0 1 0 0 0 0 10 (Direct II).

B=1 0 0 0.

C=21 2 −16 −1.

D=−2.

Figure B graphically interprets this Direct II state four-tuple S=[A,b,c,d] and its induced architecture.

Figure C shows another important IIR form, the cascade architecture. You use the basic cascade architecture to implement a transfer function of the form:

$$H(z)=K\prod_{i=1}^{Q}H_i(z). \quad \textbf{(D)}$$

Assume that $H_i(z)$ is a first- or second-order subfilter, which you define in terms of real coefficients. You define first-order subfilters in terms of real poles and zeros of H(z). You define second-order subfilters by combining

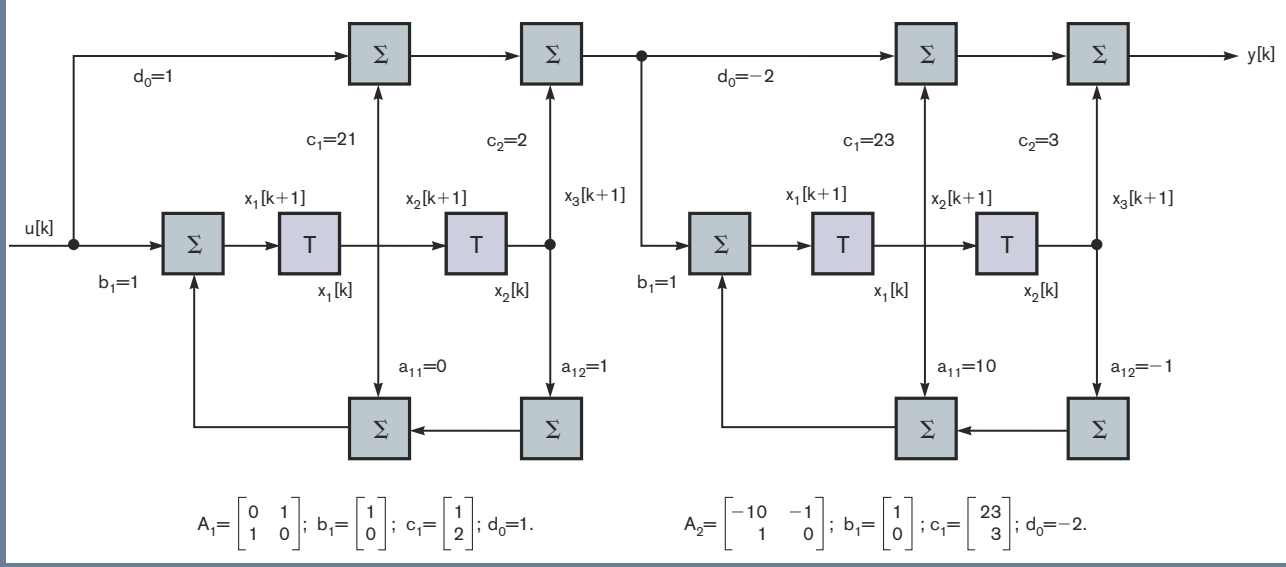


Figure D This cascade filter comprises two second-order Direct II sections.

complex poles and zeros and their complex conjugate pairs to form filter sections having only real coefficients. You can define the basic first- and second-order sections in terms of biquadratic or Direct II structures. The principal difference is that the Direct II architecture possesses a state-variable description, whereas the biquad does not. Direct II implementations have been increasingly gaining favor because of this feature.

As a general rule, filters pair zeros with the closest poles. This proximity-pairing strategy generally results in filter design that more uniformly distributes the subfilter gains across all filter sections, which is a desirable trait. Other pairing strategies can result in a few subsystems having excessively large dynamic-range requirements and others having small gains. This disparity creates a precision-allocation problem that can compromise overall system performance.

Matlab contains a collection of programs that relate to cascade-filter implementation. The function tf2sos converts digital-filter-transfer-function data to a set of second-order sections having the form:

$$\text{sos} = \begin{bmatrix} b_{01} & b_{11} & b_{21} & 1 & a_{11} & a_{21} \\ b_{02} & b_{12} & b_{22} & 1 & a_{12} & a_{22} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ b_{0L} & b_{1L} & b_{2L} & 1 & a_{1L} & a_{2L} \end{bmatrix}, \quad \textbf{(E)}$$

where the ith row of the array sos specifies the coefficients of the ith subfilter:

$$H_i(z) = K\frac{B_i(z)}{A_i(z)} = K\frac{b_{0i}+b_{1i}z^{-1}+b_{2i}z^{-2}}{a_{0i}+a_{1i}z^{-1}+a_{2i}z^{-2}}. \quad \textbf{(F)}$$

The Matlab program zp2sos converts a transfer function, H(z), in terms of its zeros, poles, and gain, into an Lx6 sos array. The program sos2ss maps second-order-filter sections into a Direct II state-space form, and the program sos2tf converts a collection of second-order-filter sections into an overall transfer function. If a filter section is first-order, the coefficients b2i and a2i are zero. Finally, the program sos2zp converts second-order-filter sections into a zero-pole-gain form.

Consider a transfer function $H(z)=H_1(z)H_2(z)$, where:

$$H(z) = \frac{-2+z^{-1}+2z^{-2}+4z^{-3}+z^{-4}}{1+10z^{-1}+0z^{-2}-10z^{-3}-z^{-4}} = H_1(z)H_2(z);$$
$$H_1(z) = \frac{1+z^{-1}+z^{-2}}{1-z^{-2}} = 1+\frac{z^{-1}+2z^{-2}}{1-z^{-2}}; \text{ and} \quad \textbf{(G)}$$
$$H_2(z) = \frac{-2+3z^{-1}+z^{-2}}{1+10z^{-1}+z^{-2}} = -2+\frac{23z^{-1}+3z^{-2}}{1+10z^{-1}+z^{-2}}.$$

You can reduce the subfilters $H_1(z)$ and $H_2(z)$ to two cascaded, second-order Direct II sections using Matlab. The Matlab representation of the filter sections is sos=[1 1 1 1 0 −1; −2 3 1 1 1 0 1]; {$H_1(z)$, $H_2(z)$}. From this database, sos2tf can map the definition of the second-order section to the original transfer function as follows:

```
sos=[1 1 1 1 0 −1; −2 3 1 1 1 0 1].
[b,a]=sos2tf(sos).
b=−2 1 2 4 1.
a=1 10 0 −10 −1.
```

The vectors b and a are the coefficients of transfer function H(z). Finally, using sos2ss, you can convert the individual second-order sections into a Direct II state-variable form:

```
sos1=[1 1 1 1 0 −1]; [A,B,C,D]=sos2ss(sos1).
```

(continued on pg 118)

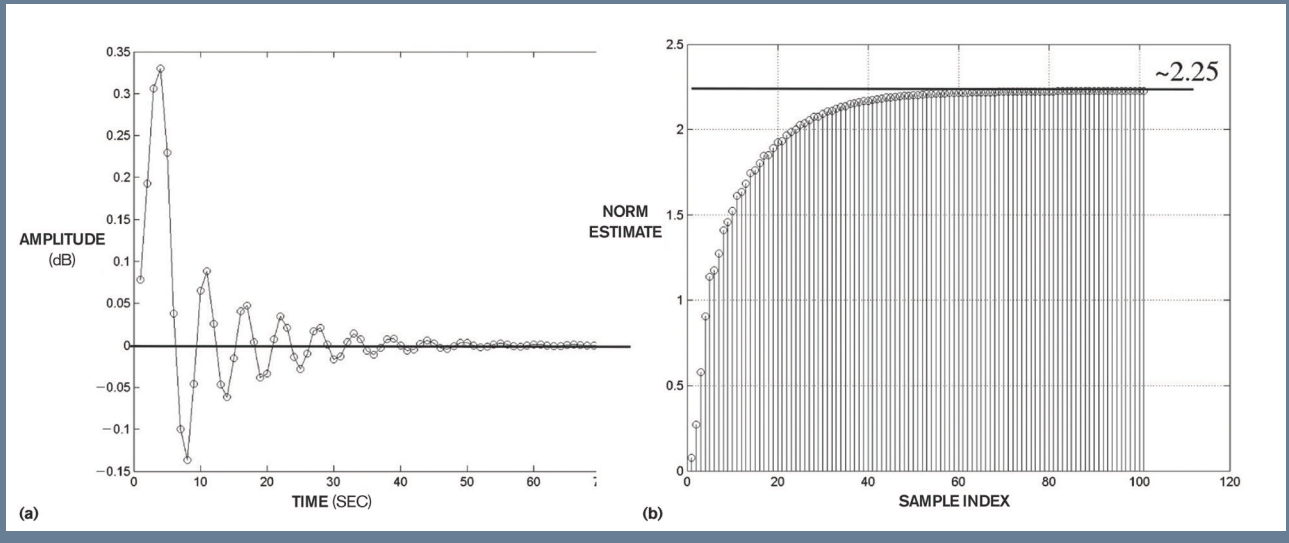
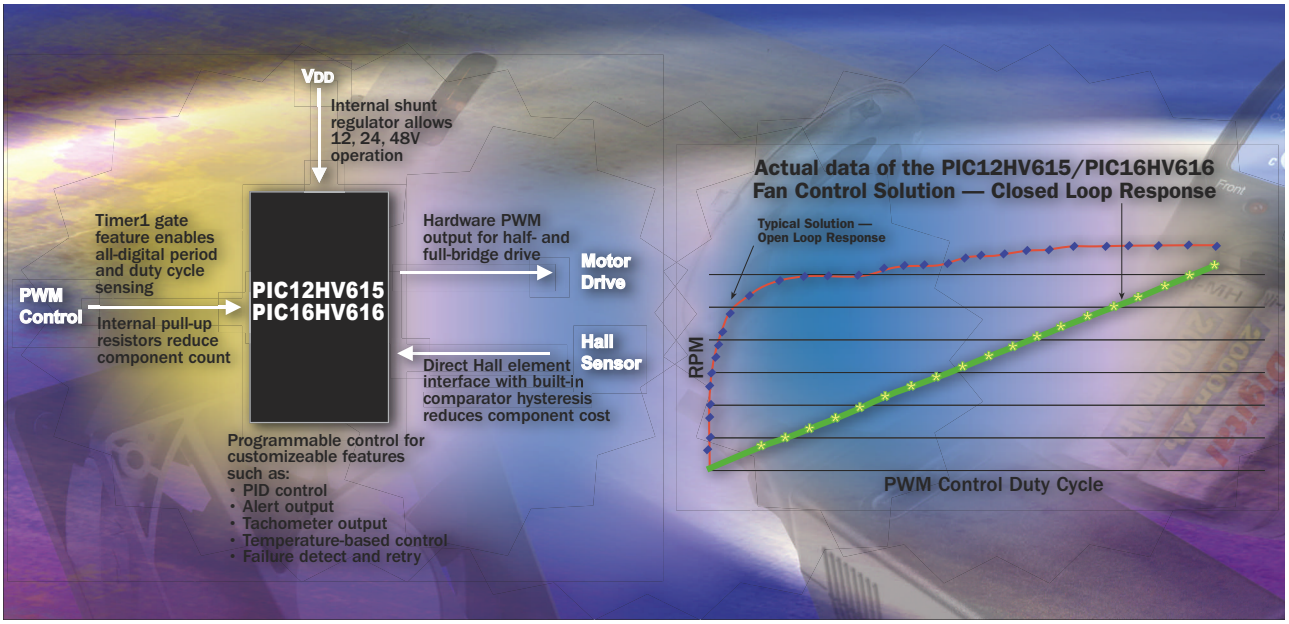


Figure E Measuring a Direct II filter's impulse response at a shift register (a) and its L_1-norm estimate (b) shows a worst-case gain of 2.25.

PIC12HV615/PIC16HV616 Closed Loop Fan Speed Control



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- Offers high voltage support with integrated shunt regulator
- User-enabled comparator for hysteresis direct interface with a Hall Element

	High Voltage Support	Program Memory	10-bit ADC (channels)	Comparators	Enhanced CCP*	Internal Oscillator
PIC12F615	—	1.75 KB/1 Kw	4	1	Half bridge	8 MHz
PIC12HV615	Yes	1.75 KB/1 Kw	4	1	Half bridge	8 MHz
PIC16F616	—	3.5 KB/2 Kw	8	2	Full bridge	8 MHz
PIC16HV616	Yes	3.5 KB/2 Kw	8	2	Full bridge	8 MHz

* Capture, Compare, PWM

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(continued from pg 116)

```
A=0 1 1 0.
B=1 0.
C=1 2.
D=1 1.
sos2=[−2 3 1 1 10 1].
[A,B,C,D]=sos2ss(sos2).
A=−10 −1 1 0.
B=1 0.
C=23 3.
D=−2.
```

Figure D shows the resultant cascade filter, comprising two second-order Direct II sections.

Using The MathWorks' FDATool (filter-design and-analysis tool), you can implement an eighth-order Chebyshev II IIR lowpass filter using a sampling frequency of 100 kHz, an attenuation frequency of 20 kHz, and a stopband attenuation of 30 dB. Using Matlab's architectural tools, you can implement the designed filter as a Direct II and cascade filter. First, compute the n-state-determined impulse-response vector and its L_1 norm, $\|h_1[k]\|_1$. Figure E shows the production of $\|h_1[k]\|_1$ for the Direct II case. You then use the state-determined impulse response to compute the worst-case gain of 2.25. Referring to Figure 2, note that all the shift registers are chained together. Therefore, the dynamic-range requirement of the first shift register is identical to that of all the other shift registers. This situation indicates that the Direct II shift registers need an additional $\log_2(2.25) \sim 1.17$ bits.

Figure F shows the L_1 norms of the state-determined impulse responses of the cascade IIR, which you can analyze and use to study the IIR. The largest L_1 norm is in the fourth subfilter and is approximately 1.8 ($\log_2(1.8) \sim 0.85$ bits), which is less than the maximal L_1 norm of the Direct II filter model.

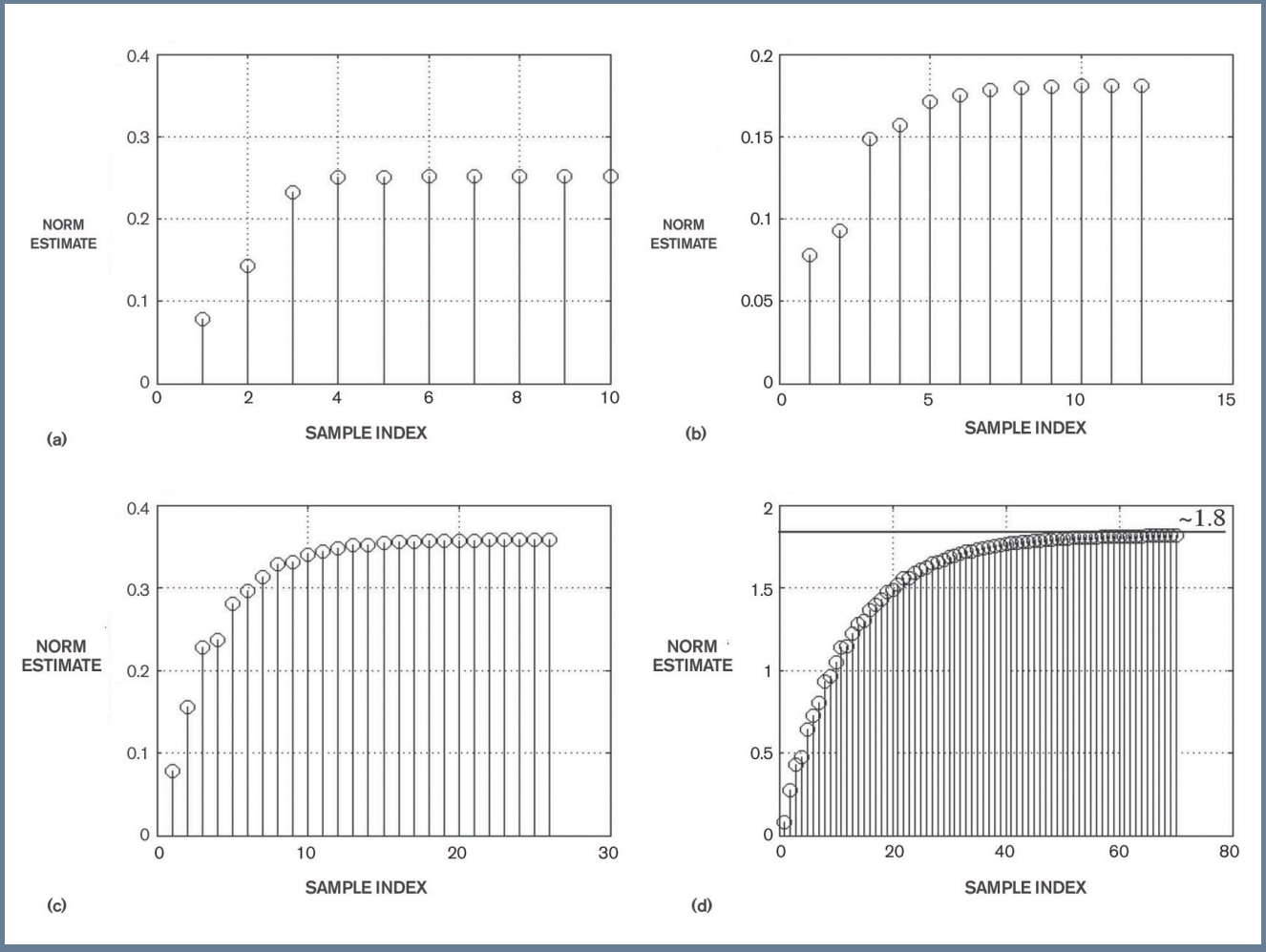

Figure F You can analyze the L_1 norms of the state-determined impulse responses of the cascade IIR to study the Direct II IIR in Stage 1 (a), Stage 2 (b), Stage 3 (c), and Stage 4 (d).

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(*continued from pg 112*)

precision registers provide additional head room that allows the filter to store and preserve a system's states without introducing saturation errors.

The ideal method of overcoming the threat of runtime overflow is to determine the worst-case filter gain, which you measure at each register or state location. Mathematically, the worst-case gain measured at the ith shift-register location is:

$$G_{MAX:i} = \sum_{m=0}^{\infty} |h_i[m]| \le 2^I, \quad (1)$$

where $h_i[m]$ is the impulse response at the output of the ith shift register—that is, the ith state location. $G_{MAX:i}$ is the L_1 norm of the ith state register. The ith state norm that **Equation 1** defines states that I integer bits of precision are necessary to ensure that the ith state does not produce a run-time-overflow error. You can generate the impulse response, $h_i[m]$, using a state-variable model and general-purpose digital computer. You define **Equation 1** in terms of a vector-valued impulse response of the form $h[m+1]=Ah[m]+b\delta[m]$, where the ith element of the n-dimensional vector, h[m], is $h_i[m]$. A potential problem, however, arises when you note that **Equation 1** requires an infinite sum, which is unrealistic. Another approach, however, is available.

You can assume that the system under study is asymptotically stable. This assumption ensures that the impulse-response vector, h[m], essentially converges to zero by a finite-sample index $m \le M$. Because M is finite, you can compute the impulse response at each shift register and attendant L_1-norm $G_{MAX:i}$ in finite time. You can use Matlab's norm function to compute the L_1 norms, which you can then use to establish the dynamic-range requirements of the state registers. The following example demonstrates this concept.

SIMULINK HOSTS A PLETHORA OF FEATURES TO SUPPORT DESIGN ANALYSIS. FIXED-POINT FILTERS, FOR EXAMPLE, OFFER A MEASURE FOR THE DYNAMIC-RANGE NEEDS FOR INTERNAL CALCULATIONS.

The source of serious arithmetic error that an IIR produces involves fixed-point MAC (multiply-accumulate) or SAXPY (S=AX+Y) calls. You can round data at a number of locations within a MAC stream. It has become commonplace to employ extended-precision accumulators that can accept full-precision products from the multiplier and sequentially accumulate the products with sufficient head room to preclude runtime-accumulator overflow. Once you have summed the full-precision products, you can then round them to the filter's basic word length—16 bits, for example. Each rounding introduces an error having a mean value of zero and a variance of $\sigma^2=Q^2/12$, where Q is the quantization-step size and has a value of $Q=2^{-F}$ and where F denotes the fractional precision you assign to a data word. For example, in a Texas Instruments' (www.ti.com) Q.15 environment, F=15 bits.

Using this model, you can theoretically predict the effect of arithmetic-rounding errors by computing the NPG (noise-power gain) between a noise-injection point and the output. The noise-injection points are normally the state registers (see **sidebar** "IIR-filter architectures" on pg 114). In this paradigm, assume that the input to the ith state register contains m_i round-off-error sources, in which each source has a mean of zero and a variance of $\sigma^2=Q^2/12$. IIR filters are so treacherous because these errors recirculate through the filter, building up noise power over time and reducing the output SNR. You can conceptually compute the noise-power gain by tracing the signal-power path between a state-shift register and the output. By defining $NPG_i, i\epsilon[1,n]$ to be the noise-power gain associated with the ith state, the output-noise error variance then becomes:

$$\sigma^2 = \frac{Q^2}{12}\sum_{k=1}^{n} m_i NPG_i = \frac{Q^2}{12}(NPG). \quad (2)$$

You can determine the filter's noise gain in bits using $NG_2=\log_2(\sqrt{NPG})$. NG_2 is an estimate of the statistical degradation of the IIR filter's output in bits due to accumulated round-off errors in the filter. In practice, you can estimate the noise-power gain using fixed-point simulation.

You can use The MathWorks' Simulink to perform an end-to-end fixed simulation of an eighth-order Chebyshev II IIR lowpass filter. The basic filter data's word length is 16 bits, and the filter comes with a full-precision multiplier and an extended-precision accumulator. A Simulink simulator tests the behavior of a 16-bit filter for fractional precisions ranging from $F\epsilon[0,15]$ (**Figure 1**). The key architectural choices defining the simulation are a data-word length, N, of 16 bits; a fractional precision of $F\epsilon[0:15]$ bits; an input-data format of $x[k]\epsilon[N:F]$ bits (N:F denotes an N-bit word with F fractional bits of precision); an output-data format of $y[k]\epsilon[N:F]$ bits; a coefficient-data format of $c_k\epsilon[N:F]$ bits; multiplier datapaths of $16\times16\rightarrow32$ bits; Direct II accumulator datapaths of $32+(32+N_{DII})\rightarrow32+N_{DII}$ bits ($N_{DII}\ge\log_2(2.25)\sim1.17$ bits; (**sidebar Figure E**, pg 116) and cascade-accumulator datapaths of $32+(32+N_C)\rightarrow32+N_C$ bits ($N_C\ge\log_2(1.8)\sim0.8$ bits) (**sidebar Figure F**, pg 118). [N:F] denotes an N-bit word with F fractional bits of precision. Assume that an extended-precision accumulator has additional head room. For the Direct II filter, the head-room requirement is $N_{DII}=2\ge\log_2(2.25)$ bits. For a cascade filter, the head-room requirement is $N_C=1\ge\log_2(1.8)$ bits. Upon accumulation, assume that data rounds to a signed 16-bit word having F fractional bits of precision, where $F\epsilon[0,15]$ bits. Simulink also hosts a plethora of features to support design analysis. Fixed-point filters, for example, offer a measure for the dynamic-range needs for internal calculations. The command sfrac(N,I) creates an N-bit structure having a signed fractional form with I integer bits. To illustrate, you can model

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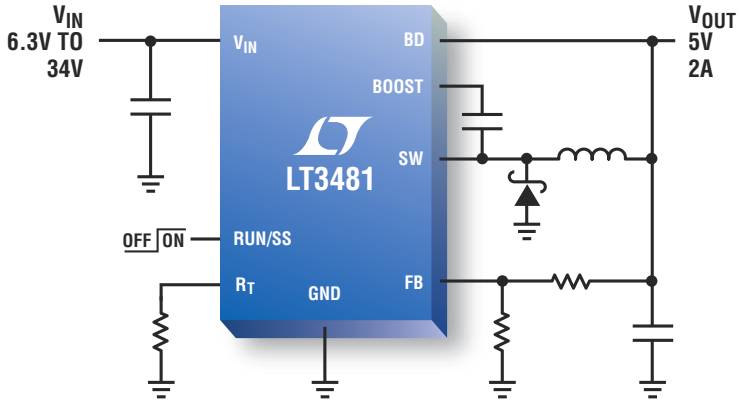

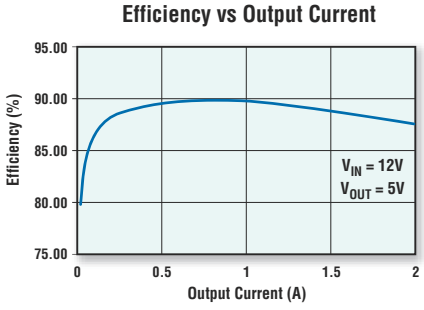

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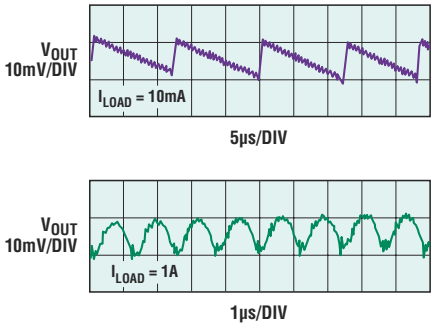

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a 16-bit system with no fractional precision using the structure sfrac(16,15). When the simulation is complete, you can use the fixed-point GUI to examine runtime-saturation effects (**Figure 2**). The input-forcing function in the example is a 2048-sample, unit-bound, uniformly distributed random signal that emulates a worst-case input.

Figure 3 shows the simulated output, from which you can partition the results as those having too little precision due to having too few fractional bits of accuracy; those in the linear regime, meaning that they have sufficient dynamic range to inhibit runtime overflow and sufficient fractional precision to eliminate traumatic round-off errors; and those having too little dynamic range due to having too few integer bits, resulting in too small a dynamic range, and ultimately resulting in a plethora of runtime-overflow errors.

The Direct II architecture exhibits overflow contamination beginning at two integer bits, as the L_1-norm analysis predicts. Similarly, as the analysis predicts, the cascade filter began exhibiting register overflow at one integer bit. Moreover, the Direct II has slightly better statistical precision than the linear input/output operating range, which the analytical study predicts. In the linear region, the analysis predicts that the cascade architecture is about 0.3 of a bit inferior to a Direct II. The simulation suggests that the optimal cascade filter should carry a [16:14] format, resulting in a solution having statistically about 11.5 fractional bits of precision. The simulation also suggests that the Direct II filter should carry a [16:13] format, resulting in a solution having statistically about 11 fractional bits of precision.

The system always used a worst-case or nearly worst-case input to mimic the most severe conditions. Analyzing the system using an impulse or sinusoidal test signal produces different, erroneous, and ultimately inconclusive results. You can predict the optimal operational point of a fixed-point IIR using simulation to produce results that are consistent with classic analytical techniques. You can exploit the existence of predefined blocks by invoking the Simulink library browser from the Launch Pad in Matlab. EDN

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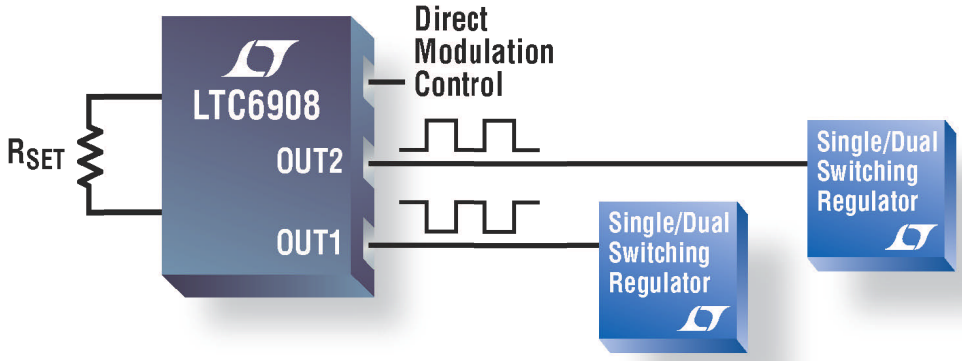

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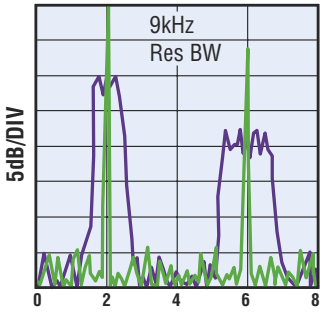

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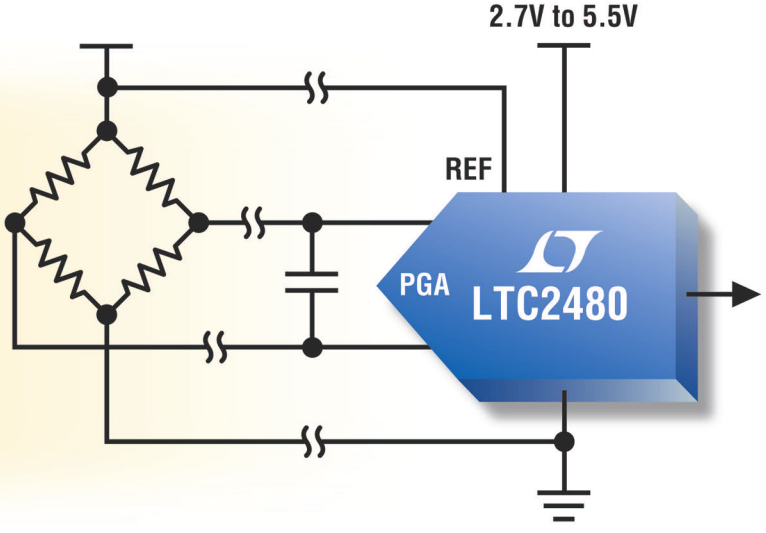

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LTC2482	16-Bits	SPI	1		7.5Hz	3mm x 3mm DFN-10	$1.65
LTC2483	16-Bits	I²C	1		7.5Hz	3mm x 3mm DFN-10	$1.65
LTC2484	24-Bits	SPI	1	Yes	7.5Hz/15Hz	3mm x 3mm DFN-10	$2.45
LTC2485	24-Bits	I²C	1	Yes	7.5Hz/15Hz	3mm x 3mm DFN-10	$2.45

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READERS SOLVE DESIGN PROBLEMS

LED senses and displays ambient-light intensity

Dhananjay V Gadre and Sheetal Vashist,
ECE Division, Netaji Subhas Institute of Technology, New Delhi, India

In addition to their customary roles as indicators and illuminators, modern LEDs can also serve as photovoltaic detectors (**references 1** and **2**). Simply connecting a red LED to a multimeter and illuminating the LED with a source of bright light, such as a similar red LED, produce a reading of more than 1.4V (**Figure 1**). One model for a reverse-biased LED comprises a charged capacitor that connects in parallel with a light-dependent current source (**Reference 1**). Increasing the incident light increases the current source and more rapidly discharges the equivalent capacitor to the supply voltage.

Figure 2 shows a method of using an LED as a photovoltaic detector. Connecting one of the microcontroller's outputs, Pin 2, to the LED's cathode applies reverse bias that charges the LED's internal capacitance to the supply voltage. Connecting the LED's cathode to Input Pin 3 attaches a high-impedance load to the LED. Illuminating the LED generates photocurrent. Originally charged to the supply voltage, the LED's internal capacitance discharges through the photocurrent source, and, when the voltage on the capacitor falls below the microcontroller's lower logic threshold voltage, Pin 3 senses a logic zero. Increasing the incident-light intensity more quickly discharges the capacitor, and lower light levels decrease the discharge rate. The microcontroller, an Atmel AVR ATtiny15 (www.atmel.com/dyn/products/product_card.asp?part_id=2033), measures the time for Pin 3's voltage to reach logic zero and computes the amount of ambient light incident on the LED. In addition, the microcontroller flashes the same LED at a frequency proportional to the incident light's intensity.

Figure 3 shows a 3-mm, superbright-red LED, D_1, from Everlight Electronics Co Ltd (www.everlight.com), which comes in a water-clear encapsulant as an ambient-light sensor. Having only four components, the circuit operates from any dc-power source from 3 to 5.5V. The circuit uses only three of six of the AVR ATtiny15's I/O pins, and the remaining pins are available to control or communicate with external devices. The sensor LED connects to the AVR microcontroller's port pins PB0 and PB1; another port pin, PB3, produces a square wave with a frequency proportional to the incident-light intensity. The circuit operates by

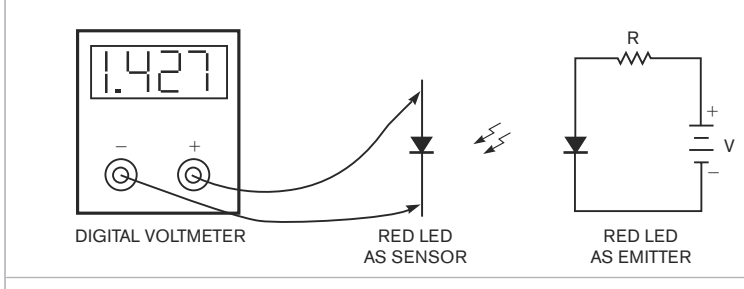

Figure 1 Two identical LEDs, closely spaced in a light-shielded housing, form a photovoltaic-characterization fixture. Choose resistor R and voltage source V to apply nominal forward current to the illuminating LED.

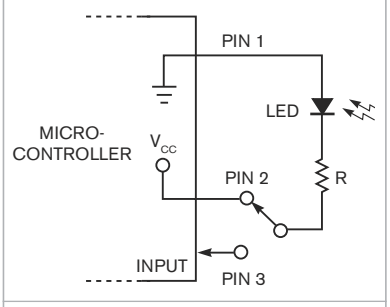

Figure 2 Connecting one of the microcontroller's outputs, Pin 2, to the LED's cathode applies reverse bias that charges the LED's internal capacitance to the supply voltage. Connecting the LED's cathode to Input Pin 3 attaches a high-impedance load to the LED. (Note that pin numbers are representative only and not actual pin numbers.)

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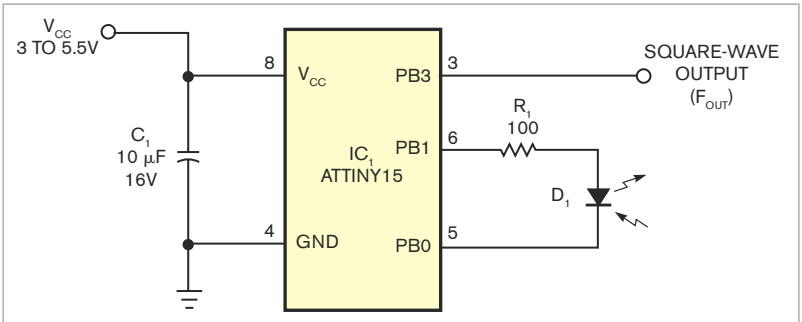

Figure 3 An LED doubles as a light-level sensor. Output PB3 delivers a square wave whose frequency increases as light intensity increases.

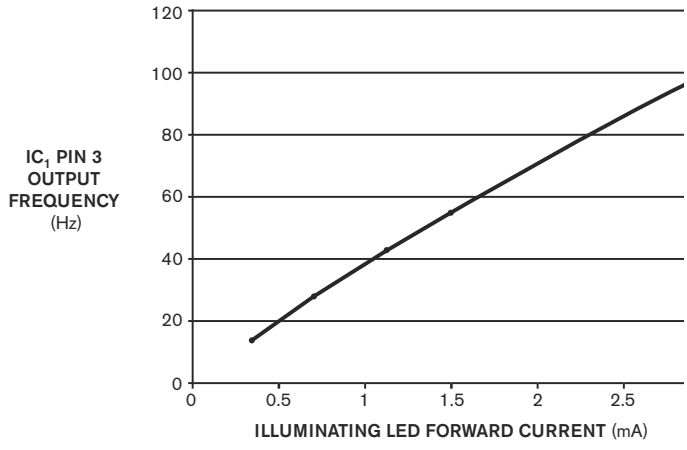

Figure 4 The frequency of the circuit's square-wave output exhibits good linearity versus light level for identical sensor and source LEDs.

first applying forward bias to the LED for a fixed interval and then applying reverse bias to the LED by changing the bit sequences you apply to PB0 and PB1. Next, the microcontroller reconfigures PB0 as an input pin. An internal timing loop measures the interval, T, for the voltage you apply to PB0 to decrease from logic one to logic zero.

Reconfiguring pins PB0 and PB1 to apply forward bias to the LED completes the cycle. Time interval T varies inversely with the amount of ambient light incident on the LED. For lower light, the LED flashes at a lower frequency, and, as the incident-light intensity increases, the LED flashes more frequently to provide a visual indication of the incident-light intensity.

For low values of forward current, an LED's light-output intensity is fairly linear (**Reference 2**). To test the circuit, couple the light output of a second and identical LED to the sensor LED, D_1, in **Figure 3**. Ensure that external light doesn't strike the sensor LED by enclosing the LEDs in a sealed tube covered with opaque black tape. Varying the illuminating LED's forward current from 0.33 to 2.8 mA produces a relatively linear sensor-flash-frequency plot (**Figure 4**).

The efficiency of an LED as a sensor depends upon its reverse-biased internal-current source and capacitance. To estimate the reverse photocurrent, connect a 1-MΩ resistor in parallel with a sensor LED and measure the voltage across the resistor while applying a constant level of illumination from an external source. Replace the 1-MΩ resistor with 500- and 100-kΩ resistors and repeat the measurements. For a representative LED under constant illumination and shielded from stray ambient light, we measured a photocurrent of approximately 25 nA for all three resistor values. For the same level of illumination applied to the sensor LED, measure the frequency generated at Pin PB3.

To calculate the LED's reverse-biased capacitance, substitute the delay-loop time, the LED's photovoltaic current, and the microcontroller's logic-one and -zero threshold voltages into the equation and solve for C, the LED's effective reverse-biased junction capacitance: (dV/dt)=(I/C), where dV is the measured logic-one voltage minus the logic-zero voltage, dt is the measured time to discharge the LED's internal capacitor, and I is the calculated value of LED's photocurrent source. The calculated values for the selected LED range from 25 to 60 pF. This range compares with the data in **references 3** and **4**, although **Reference 3** reports only the current source's values. You can download the AVR microcontroller's assembly-language firmware, **Listing 1**, from this Design Idea's online version at www.edn.com/061109di1.EDN

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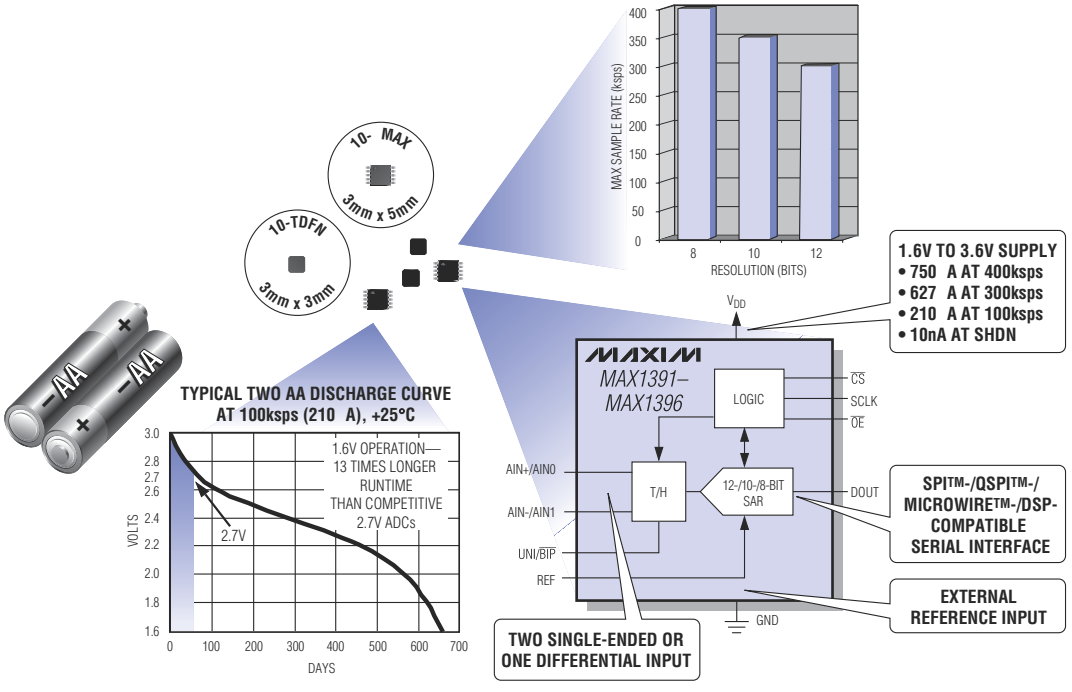

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AC line powers microcontroller-based fan-speed regulator

Abel Raynus, Armatron International Inc, Malden, MA

A microcontroller requires dc operating power in the 2 to 5.5V range, an amount that a battery or a secondary power source can easily supply. However, in certain situations, a microcontroller-based product must operate directly from a 120 or 220V-ac power outlet without a step-down transformer or a heat-producing, voltage-decreasing resistor. As an alternative, a polyester/polypropylene film capacitor rated for ac-line service can serve as a nondissipative reactance (**Figure 1**). Capacitor C_1, a 2-µF AVX (www.avxcorp.com) FFB16C0205K rated for 150V rms, provides a significant ac-voltage drop that reduces the voltage you apply to a diode-bridge rectifier, D_1. A flameproof metal-film resistor, R_1, limits current spikes and transient voltages induced in the ac-power line by lightning strikes and abrupt load changes. In this application, the ac current does not exceed 100 mA rms, and a 51Ω, 1W resistor provides adequate current limiting. R_2, a 5W, 160Ω Yageo (www.yageo.com) type-J resistor, and D_2, a 1N4733A zener diode, provide 5V regulated power for the microcontroller, a Freescale (www.freescale.com) C68HC908QT2.

The schematic shows a representative circuit for a microcontroller-based fan-speed regulator in which a thermistor senses air temperature and the microcontroller drives a

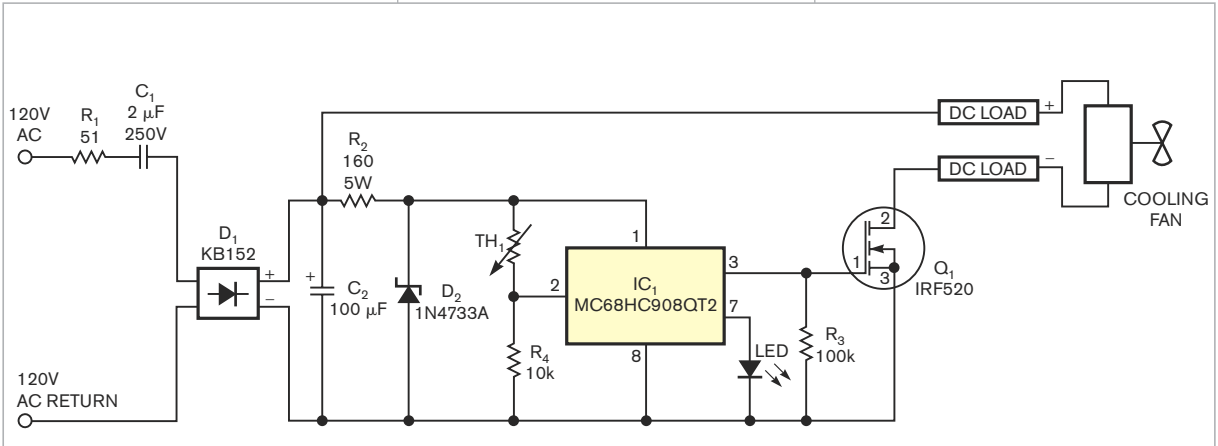

Figure 1 C_1 provides capacitive reactance, which limits ac-input current without dissipating excessive heat in this dc fan-speed controller.

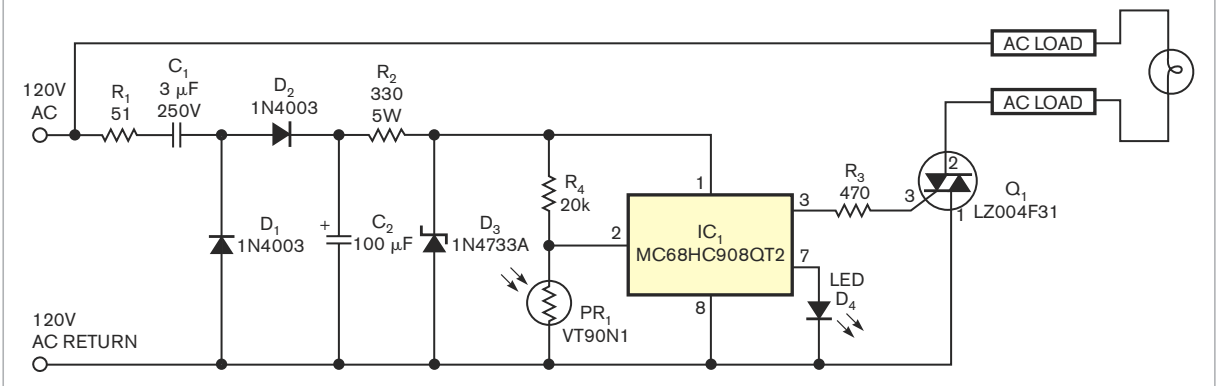

Figure 2 A two-diode rectifier and lamp-control bidirectional thyristor share a common return path to the ac line.

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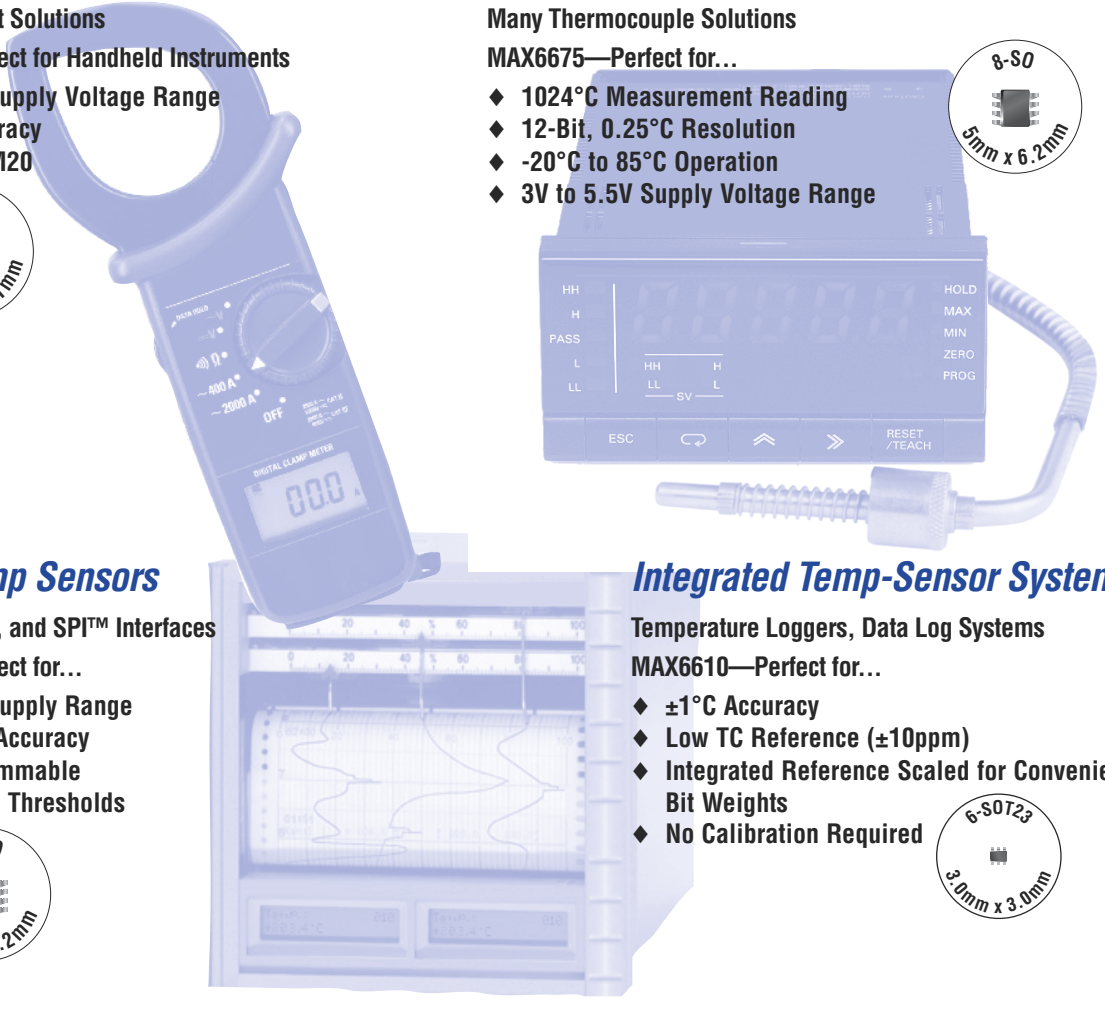

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fan's motor. **Figure 2** illustrates a light-intensity regulator based on an inexpensive two-diode rectifier and a bidirectional-thyristor-lamp controller that share a common ground. IC_2, a Fairchild (www.fairchildsemi.com) MOC3021-M bidirectional-thyristor-driver optoisolator, separates the lamp-return path from the microcontroller's ground return (**Figure 3**). In each of the three circuits, the Kingbright (www.kingbright.com) W934GD5V0 LED indicator includes a built-in current-limiting resistor (not shown).EDN

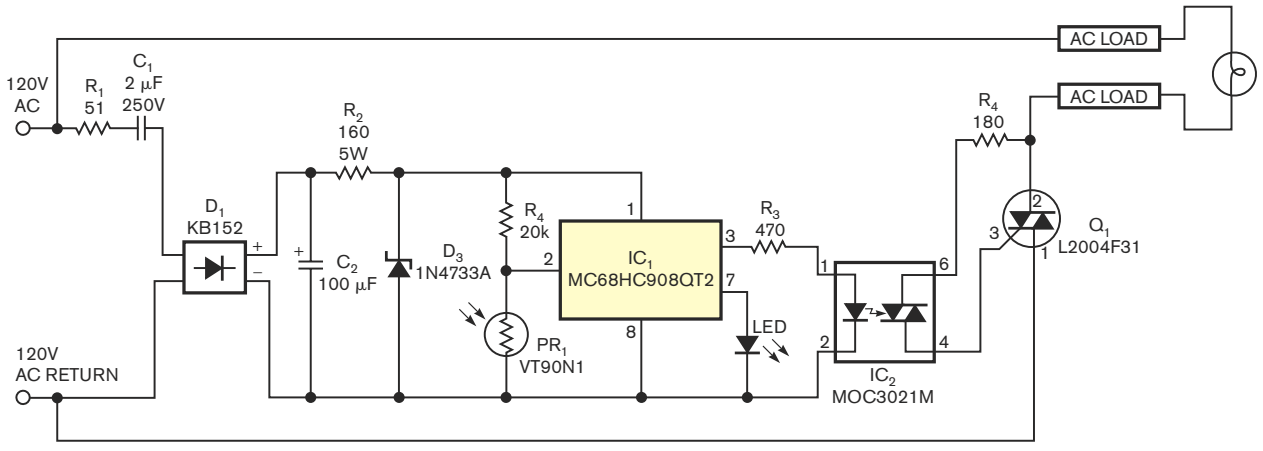

Figure 3 An optoisolator separates the bidirectional thyristor's high-current ac-line return path from the microcontroller's power supply.

Simple circuits sort out the highest voltage

Ezio Rizzo, Nova SNC, Genoa, Italy, and
Vincenzo Pronzato, Felmi SRL, Genoa, Italy

In a water-cooled power converter, analog-output sensors measure the cooling water temperature at three locations. If any of the three temperatures rises above a preset threshold, an alarm sounds and attracts the attention of the system's operator. When the alarm activates, knowing which measurement site has reached the highest temperature saves troubleshooting time and prevents system damage. The circuit in **Figure 1** delivers an analog-output voltage equal to the highest of three input voltages that drives a display for continuous temperature monitoring. LED indicators identify which of three sensors shows the highest temperature. An external adjustable-threshold comparator (not shown) monitors the analog-voltage output and activates an audible alarm.

Each of three analog input signals spans a range of 0 to 10V. Driven by the highest-voltage input, which you apply at IN_1 in this example, operational amplifier IC_{1A} functions as a voltage follower with diode D_1 in its feedback path. The op amp's open-loop gain divides the diode's forward-voltage drop to a fraction of its nominal value, producing an "ideal diode" with a voltage drop of millivolts.

THE CIRCUIT DELIVERS AN ANALOG-OUTPUT VOLTAGE EQUAL TO THE HIGHEST OF THREE INPUT VOLTAGES THAT DRIVES A DISPLAY FOR CONTINUOUS TEMPERATURE MONITORING.

Op amps IC_{1B} and IC_{1C} function as high-input-impedance inverting comparators. Each "sees" the highest input voltage on its inverting input and one of two lower input voltages, IN_2 and IN_3, on its noninverting input and delivers an output voltage near that of the negative-supply-voltage rail. Thus, only IC_{1A} delivers a positive-voltage output to MOSFET Q_1's gate, and IC_{1B} and IC_{1C} deliver negative outputs to the gates of Q_2 and Q_3. Q_1 turns on, lighting LED D_4 and drawing approximately 5 mA to develop 11V across R_3, which guarantees that Q_2 and Q_3 and their corresponding LEDs remain off. The voltage that develops across R_1 represents the largest voltage of the three inputs, and resistor R_4 and

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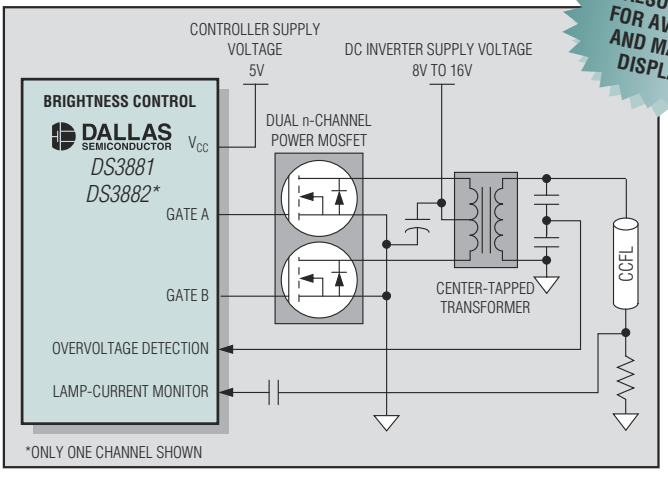

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capacitor C_1 form a lowpass filter that reduces high-frequency noise that the sensor cables pick up. Voltage follower IC_{1D} buffers the filter's output voltage. **Figure 2** (pg 136) shows the results of an LTSpice simulation featuring three sinusoidal inputs and the resultant analog output summed with a small dc-offset voltage for clarity.

The breadboarded circuit works as designed. Given its electrically noisy location near a 300-kHz, 30-kW switched-mode power converter, it uses slow-switching 1N4004 diodes to avoid malfunctions, which the rectification of stray high-frequency interference introduces. In less noisy environments, use any small-signal diode whose peak-inverse voltage exceeds at least 30V. Most varieties of operational amplifiers work well in the circuit, but for greater high-frequency immunity, use a JFET-input quad op amp, such as Texas Instruments' (www.ti.com) TL084.

Although the circuit's prototype uses red-LED indicators, LEDs of other colors work well. To change the LEDs' current to another value, change the values of R_2 and R_3, keeping approximately the same 3-to-2 ratio. For example, values of 1.8 kΩ for R_2 and 1.2 kΩ for R_3 drive the "on" LED with approximately 10 mA. If you increase the LED current, note that the resistors continuously dissipate power. For greatest reliability, choose resistors rated for twice the calculated power dissipation. EDN

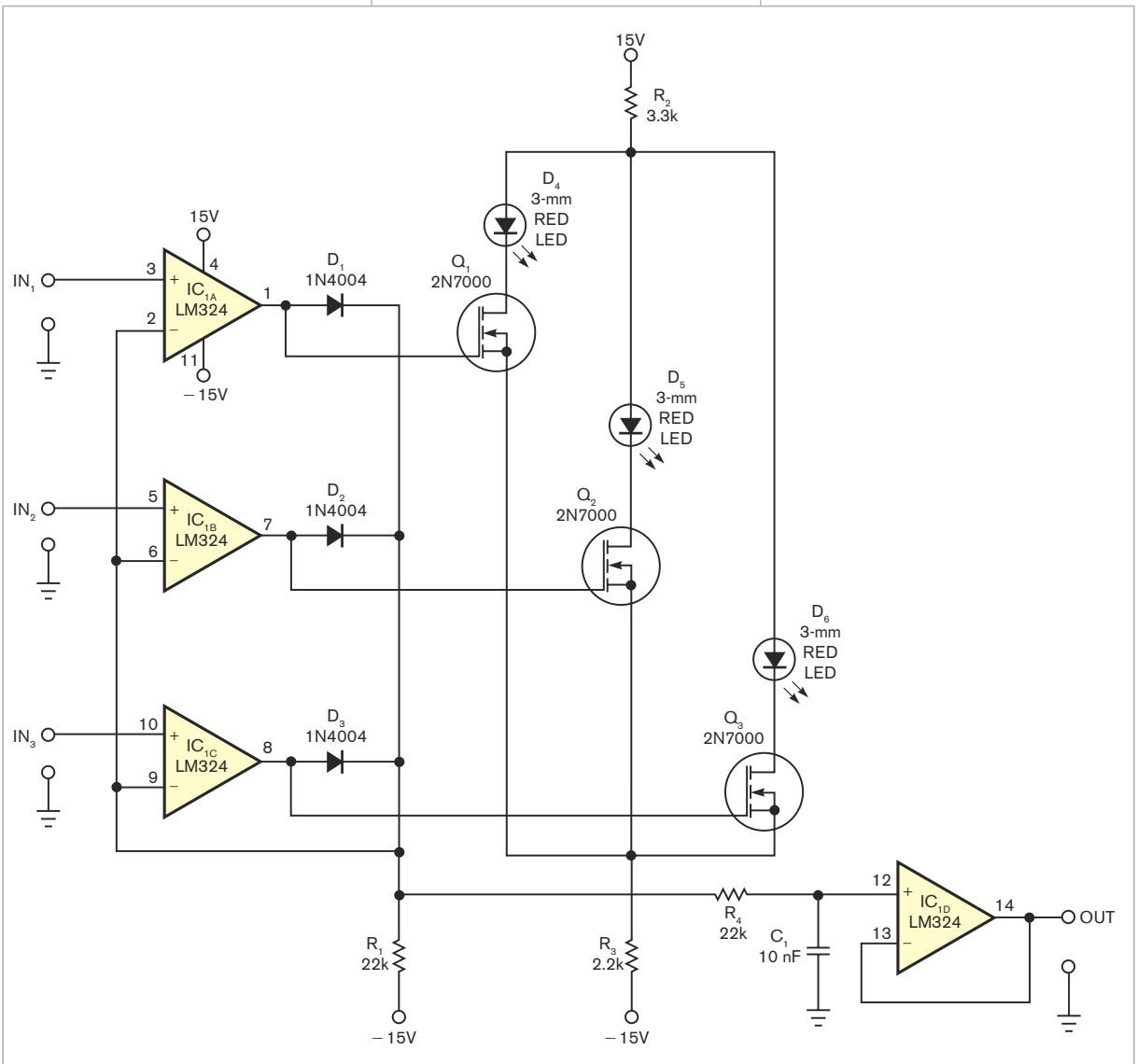

Figure 1 This circuit's output voltage tracks and indicates the highest of three input voltages and can drive an external strip-chart recorder or alarm comparator.

LINEAR TECHNOLOGY

DESIGN NOTES

Electronic Circuit Breaker in Small DFN Package Eliminates Sense Resistor – Design Note 402

SH Lim

Introduction

Traditionally, an Electronic Circuit Breaker (ECB) comprises a MOSFET, a MOSFET controller and a current sense resistor. The LTC®4213 does away with the sense resistor by using the $R_{DS(ON)}$ of the external MOSFET. The result is a simple, small solution that offers a significant low insertion loss advantage at low operating load voltage. The LTC4213 features two circuit breaking responses to varying overload conditions with three selectable trip thresholds and a high side drive for an external N-channel MOSFET switch.

Overcurrent Protection

The SENSEP and SENSEN pins monitor the load current via the $R_{DS(ON)}$ of the external MOSFET and serve as inputs to two internal comparators—SLOWCOMP and FASTCOMP—with trip points at V_{CB} and $V_{CB(FAST)}$, respectively. The circuit breaker trips when an overcurrent fault causes a substantial voltage drop across the MOSFET. An overload current exceeding $V_{CB}/R_{DS(ON)}$ causes SLOWCOMP to trip the circuit breaker after a 16µs delay. In the event of a severe overload or short-circuit current exceeding $V_{CB(FAST)}/R_{DS(ON)}$, the FASTCOMP trips the circuit breaker within 1µs, protecting both the MOSFET and the load.

Both of the comparators have a common mode input voltage range from ground to V_{CC} + 0.2V. This allows the circuit breaker to operate as the load supply turns on from 0V.

Flexible Overcurrent Setting

The LTC4213 has an I_{SEL} pin to select one of these three overcurrent settings:

I_{SEL} at GND, V_{CB} = 25mV and $V_{CB(FAST)}$ = 100mV

I_{SEL} left open, V_{CB} = 50mV and $V_{CB(FAST)}$ = 175mV

I_{SEL} at V_{CC}, V_{CB} = 100mV and $V_{CB(FAST)}$ = 325mV

Overvoltage Protection

The LTC4213 can provide load overvoltage protection (OVP) above the bias supply. When $V_{SENSEP} > V_{CC} + 0.7V$ for 65µs, an internal OVP circuit activates with the GATE pin pulling low and the external MOSFET turning off. The OVP circuit protects the system from an incorrect plug-in event where the V_{IN} load supply is much higher than the V_{CC} bias voltage.

Typical Electronic Circuit Breaker (ECB) Application

Figure 1 shows the LTC4213 in a dual supply ECB application. An input bypass capacitor is recommended to prevent transient spikes when the V_{IN} supply powers-up or the ECB responds to overcurrent conditions. Figure 2 shows a normal power-up sequence. The LTC4213 exits reset mode once the V_{CC} pin is above the internal under voltage lockout threshold and the ON pin rises above 0.8V (see trace 1 in Figure 2). After an internal 60µs debounce cycle, the GATE pin capacitance is charged up from ground by an internal 100µA current source (see trace 2). As the GATE pin and the gate of MOSFET charges up, the external MOSFET turns on when V_{GATE} exceeds the MOSFET's threshold. The circuit breaker is armed when V_{GATE} exceeds ΔV_{GSARM}, a voltage at which the external MOSFET is deemed fully enhanced and $R_{DS(ON)}$

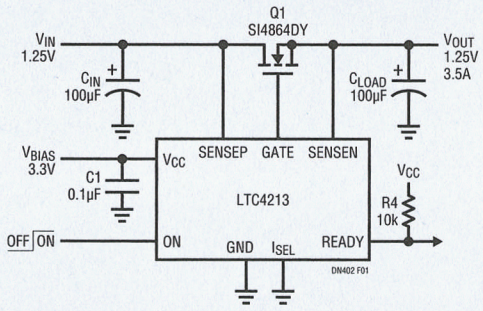

Figure 1. The LTC4213 in an Electronic Circuit Breaker Application

minimized. Then, 50µs after the circuit breaker is armed, the READY pin goes high (see trace 3) and signals the system to power up V_{IN}. Trace 4 shows the related V_{OUT} waveform when V_{IN} powers up. In order to not trip the circuit breaker during startup, the load current must be lower than V_{CB}/R_{SENSE}. If needed, the I_{SEL} pin can be stepped dynamically for a higher overcurrent threshold at startup and a lower threshold when the load current has stabilized.

Accurate ECB with Sense Resistor

The $R_{DS(ON)}$ voltage drop sensing method trades the circuit breaker accuracy for system simplicity. The majority of sensing inaccuracy is due to the external MOSFET's $R_{DS(ON)}$ varied by operating temperature and under different V_{GS} bias condition. The MOSFET vendors also do not specify the $R_{DS(ON)}$ distribution tightly due to manufacturing variation. If an external tight tolerance resistor is employed for current sensing instead, the LTC4213 reveals its ±10% circuit breaker accuracy. Figure 3 shows a tolerable R_{SENSE} resistor voltage drop and the LTC4213 is used for accurate ECB applications.

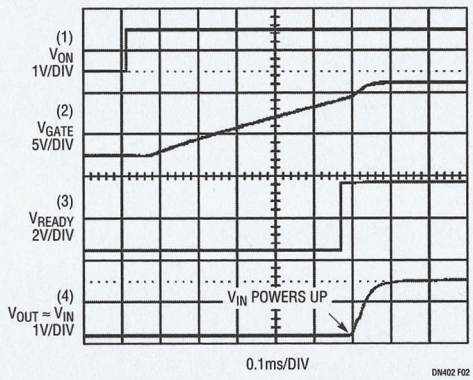

Figure 2. Normal Power-Up Sequence

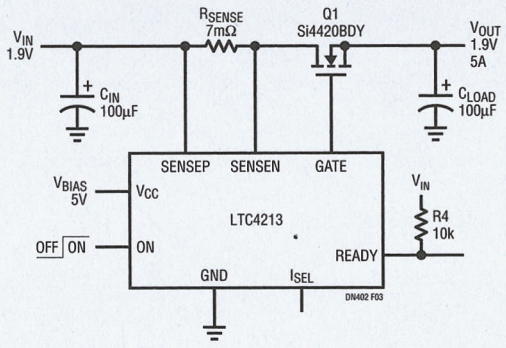

Figure 3. Accurate ECB with High Side Sense Resistor

High Side Switch for N-Channel Logic Level MOSFET

Logic level N-Channel MOSFET applications usually required a minimum gate drive voltage of 4.5V. Figure 4 shows the LTC4213 in a High Side Switch application. The LTC4213's internal charge pump boosts the GATE above the logic level gate drive requirement and ensures the MOSFET is fully enhanced for $V_{CC} \geq 3V$. The typical gate drive versus bias supply voltage curve is shown in Figure 5.

Conclusion

The LTC4213 is a small package, No R_{SENSE} Electronic Circuit Breaker that is ideally suited for low voltage applications with low MOSFET insertion loss. It includes selectable dual current level and dual response time circuit breaker functions. The circuit breaker has wide operating input common-mode-range from ground to V_{CC}.

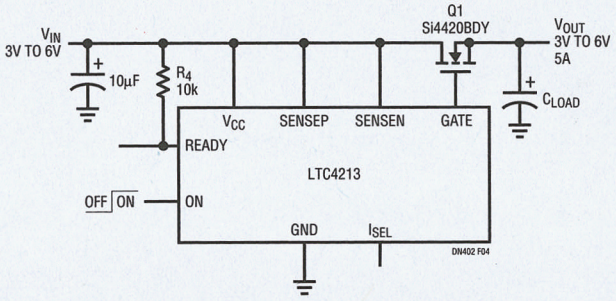

Figure 4. High Side Switch for Logic Level N-Channel MOSFET, V_{CC} > 3V

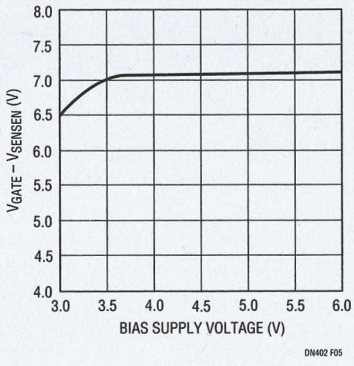

Figure 5. Gate Drive Voltage vs Bias Supply Voltage

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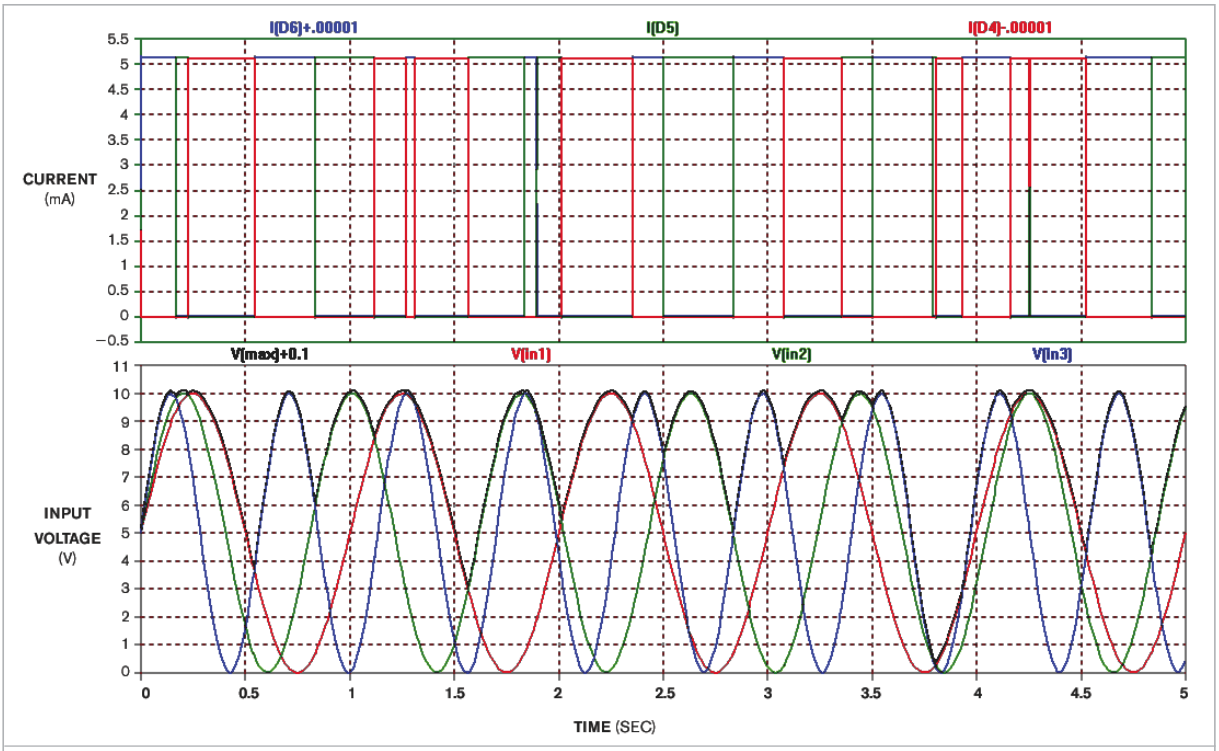

Figure 2 Three sine waves of different frequencies provide input voltages (lower traces) that evoke the greatest-of-three response in the current through R_2 (top trace, in which colored horizontal segments match the largest inputs).

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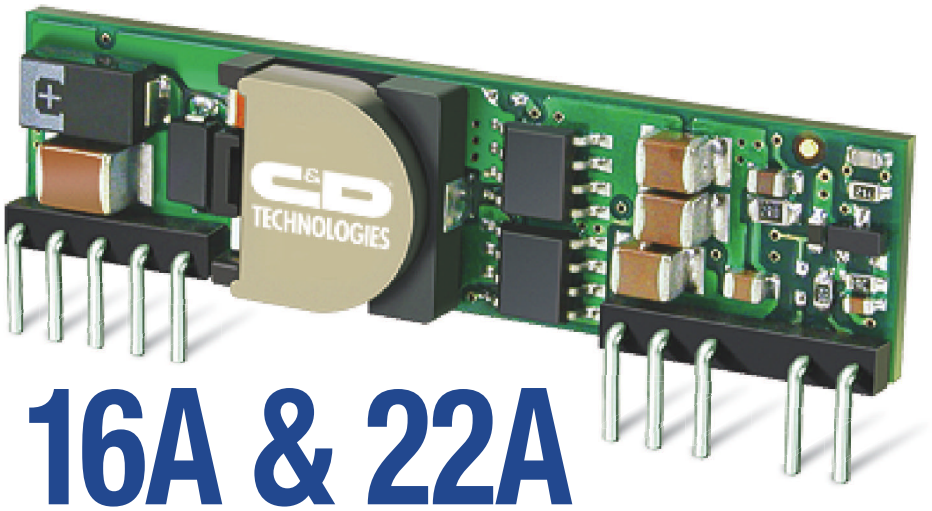

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6	12	8.3 to 14	0.75 to 5	±2	25	93		**LSN2-T/6-D12**
10	3.3	3 to 3.6	1 to 2.5	±1	35	90.5 to 95.5		**LSN-10A, D3**
10	5	2.4 to 5.5	0.75 to 3.3	±2	25	95		**LSN2-T/10-W3**
10	5	4.5 to 5.5	1 to 3.8	±1	35	89 to 96		**LSN-10A, D5**
10	12	8.3 to 14	0.75 to 5	±2	75	95		**LSN2-T/10-D12**
10	12	10.8 to 13.2	1 to 5	±1.25	45 to 75	86 to 95.5		**LSN-10A, D12**
16	5	2.4 to 5.5	0.75 to 3.3	±2	50	95		**LSN2-T/16-W3**
16	3.3/5	3 to 5.5	0.75 to 3.3	±1.5	50	86 to 95		**LSN-16A, W3**
16	12	8.3 to 14	0.75 to 5	±2	75	94		**LSN2-T/16-D12**
16	12	10 to 14	0.75 to 5	±1.25	45 to 75	86 to 95.5		**LSN-16A, D12**
22	12	8.3 TO 14	0.75 to 5	±2	90	95		**LSN2-T/22-D12**

For full specifications, options and part numbers, please download datasheets at www.cd4power.com

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productroundup

CONNECTORS

Sensor-distribution boxes come with or without molded cables

Available with four, six, or eight ports and with or without a molded cable, these sensor-distribution boxes also come in M8- and M12-connector sizes. The boxes come with a molded PUR main cable or a cable for field wiring directly to the box. Molded-cable versions come in 5, 10, and 15m lengths. Prices for the sensor-distribution boxes range from $95 to $210.
Automation Systems Interconnect, www.asi-ez.com

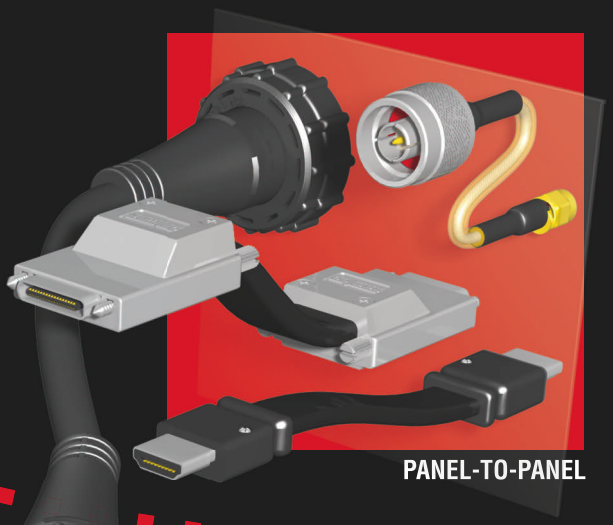
Attenuator provides optical-power control

Based on nanoparticle technology, these dynamic attenuators feature optical-power-control technology in an LC-plug-style attenuator housing. The device controls optical power by limiting or clamping it at preset values, reducing optical-power spikes and keeping improperly set power levels from damaging sensitive receivers and equipment. Able to replace fixed attenuators, these devices provide flexible and additional protection during field installations. Additional features include a mechanical housing with an internally spring-loaded ferrule assembly that protects non-spring-loaded interfaces, a thumb latch for easier removal, and a housing that fits and mates with simplex or duplex LC adapters and connectors. The attenuators cost $80 (1000).
Molex, www.molex.com

BGA packaging prevents content piracy

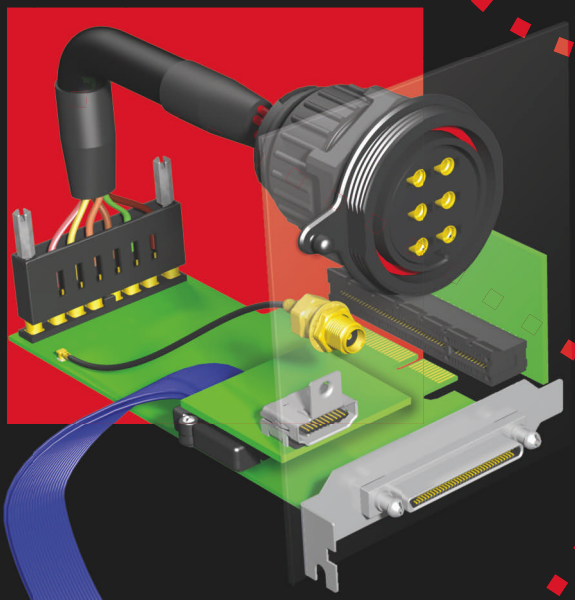
Using no exposed conductors makes the CHC series BGA-termination network less susceptible to content piracy and probing after mounting. Features include a 10Ω to 10-kΩ resistance with a ±1% absolute tolerance, a ±100ppm/°C absolute TCR (temperature coefficient of resistance), and a 25V operating voltage. The device has a 100-mW element-power rat-

SIGNAL INTEGRITY FROM THE OUTSIDE IN

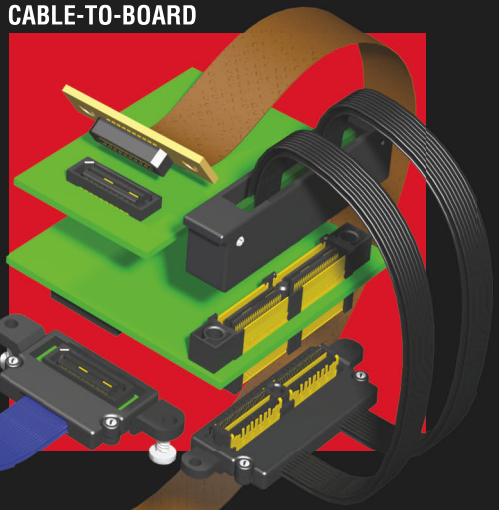


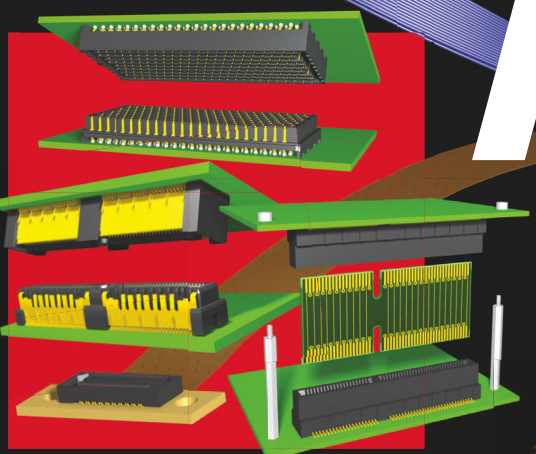
PANEL-TO-PANEL

PANEL-TO-BOARD



CABLE-TO-BOARD





BOARD-TO-BOARD

samtec

www.samtec.com/si

CONNECTORS

ing at 70°C with 1.6W package power ratings at 70°C. Targeting consumer-electronics applications, the CHC series devices cost $1 (10,000).
IRC, www.irctt.com

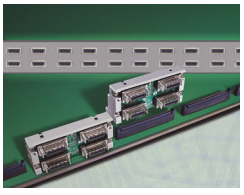
Hybrid coupler has a small package

Covering the 900- to 2500-MHz range, the high-power Model IPP-2033 90° hybrid coupler combines two 150W CW (continuous-wave) signals of total power. Features include a 0.3-dB insertion loss, less than ±5° phase balance, less than 1.30-to-1 VSWR (voltage-standing-wave ratio), less than ±0.90-dB amplitude balance, and 18-dB isolation. Available in a miniature drop-in-style package measuring 1.3×0.25×0.2 in. with solder-tab connections, the Model IPP-2033 costs $17.50 (1000).

Innovative Power Products, www.innovativepp.com

I/O-connector module provides high-speed signal transmissions

Part of the vendor's Multi-IO microGiGaCN series, the FCN-268-Y032-A connector modules accommodate five modules for a total of 20 links, in a 1U configuration on a motherboard. Suiting high-speed-signal transmission, the 2×2-stacked module of four 4× links supports InfiniBand, InfiniBand DDR, 10G fiber channel, and 10GBase-CX4 data rates in a four-channel, bidirectional data-transfer mode. The device has a 30V-ac rating, a 240-mΩ signal-contact resistance, a 180-mΩ ground-contact resistance, and a 100Ω±10% differential characteristic with 100-psec rise time. The FCN-268Y032-A module costs $37.50 (1000), and the high-speed interface connector costs $7.39 (1000).



Fujitsu Components America, www.fujitsu.com

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A. Total no. copies (net press run)	**116,733**	**116,758**
B. Legitimate paid and/or requested distribution (by mail or outside the mail)		
1. Individual paid/requested subscriptions stated on PS Form 3541	109,756	109,750
2. Copies requested by employers for distribution to employees by name or position stated on PS Form 3541	None	None
3. Sales through dealers and carriers, street vendors, counter sales and other paid or requested distribution outside USPS	4,679	4,736
4. Requested copies distributed by other mail classes through the USPS	None	None
C. Total paid and/or requested circulation	**114,435**	**114,486**
D. Nonrequested free distribution (by mail and outside the mail)		
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3. Nonrequested copies distributed outside the mail	137	None
E. Total nonrequested distribution (sum of 15D 1, 2, and 3)	**1,077**	**940**
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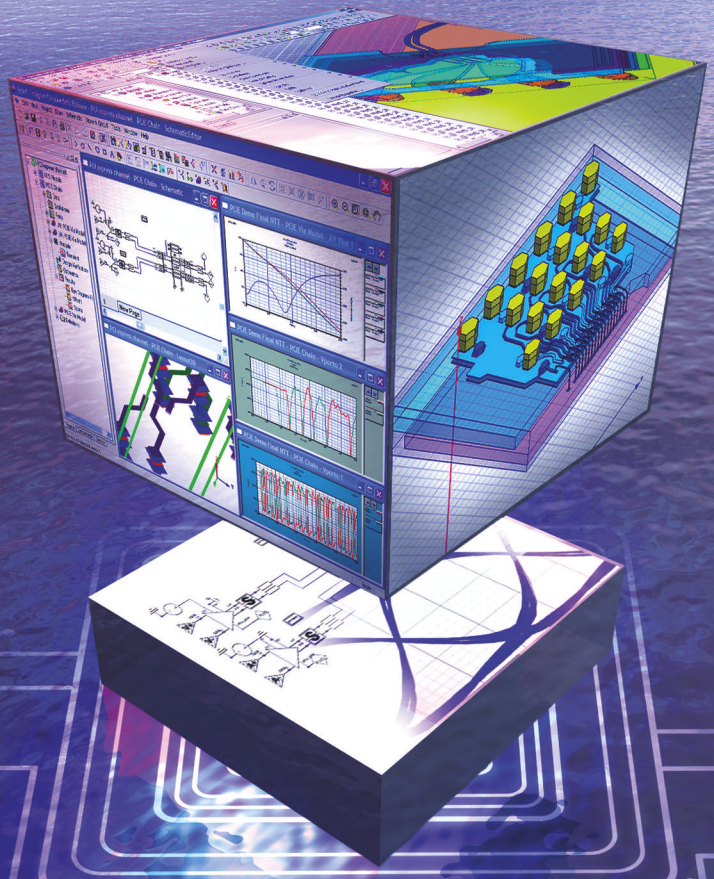

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LOOKING AHEAD

TO THE INTERNATIONAL ELECTRON DEVICES MEETING

Convening in San Francisco on Dec 11 through 13 and arguably the world's foremost conference on devices that modulate electron flow—ranging from power transistors to self-assembling nanodevices—IEDM will once again attract the who's who of device developers and researchers from around the world. Plenary topics will include a University of Michigan (www.umich.edu) presentation on breakthroughs in applying wireless technology to health care, a Philips Research (www.research.philips.com) session on the challenge of analog design in nanometer CMOS, and a look by Samsung (www.samsung.com) into the fusion of information, biotechnology, and nanotechnology into a single, financially viable discipline.

LOOKING BACK

50 YEARS AGO IN *EDN*

Transistors make it to radio frequencies

A new technique produces ultrahigh-frequency transistors. The surface-barrier-diffused transistor (SBDT) will operate in the ultrahigh-frequency range of 500 Megacycles. To make the devices, tiny germanium-transistor blanks are subjected to a high-temperature, carefully controlled atmosphere containing metal particles in gaseous form. When carefully controlled, particles of the metal penetrate the surface of the germanium by diffusion. Using mechanized precision etching, the technique can produce transistors having alpha cutoff frequencies above 600 Megacycles.

—November 1956

LOOKING AROUND

Inside the trend toward media in everything

It seems that everything—from your cell phone to your car to your washing machine—must have Internet connectivity for video-playback capability these days. But just adding video can come at a surprising cost. We are starting to see a new generation of microcontrollers for these video-capable embedded systems, and they starkly differ from the traditional architectures. Multilevel fast buses, elaborate buffering schemes, and DMA controllers that are processors in their own right all try to cope with the bandwidth and latency demands of audio and video. You don't just run HDTV through the programmable I/O on an 8051.

MC1321x ZigBee™ Family

Low power 2.4GHz radio frequency transceiver and 8-bit microcontroller in a 9x9x1mm 71-pin LGA package. Provides up to 60KB of Flash memory and 4KB of RAM. Supports star, mesh, and cluster tree networks.

freescale semiconductor mouser.com/freescale/a

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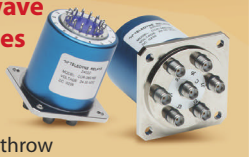
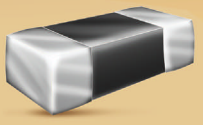
RF and Microwave Coaxial Switches



CCR-33 and CR-33 Series of failsafe, latching, and multi-throw coaxial switches. Operates from DC-18GHZ or DC-22Ghz, 50 ohms, broadband, SPDT, electromechanical. Designed to switch a microwave signal from a common input to either of two outputs.

TELEDYNE RELAYS A Teledyne Technologies Company mouser.com/teledyne/a

Multilayer Chip Inductors – LK Series



Internal printed coil structure creates a closed magnetic circuit that eliminates crosstalk and allows for higher mounting densities. Rated current 25mA, DC resistance 1.50, temp. range -40°C to +85°C, self-resistant frequency 120MHz.

KEMET CHARGED. mouser.com/kemet/a

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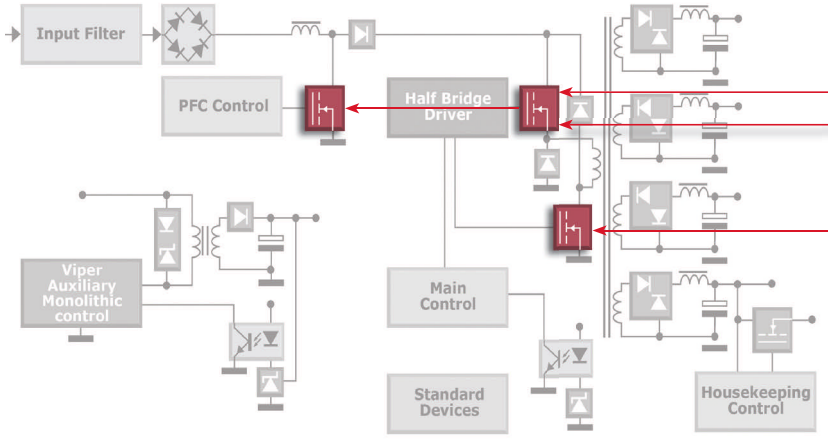
Innovative products for multi-segment application systems



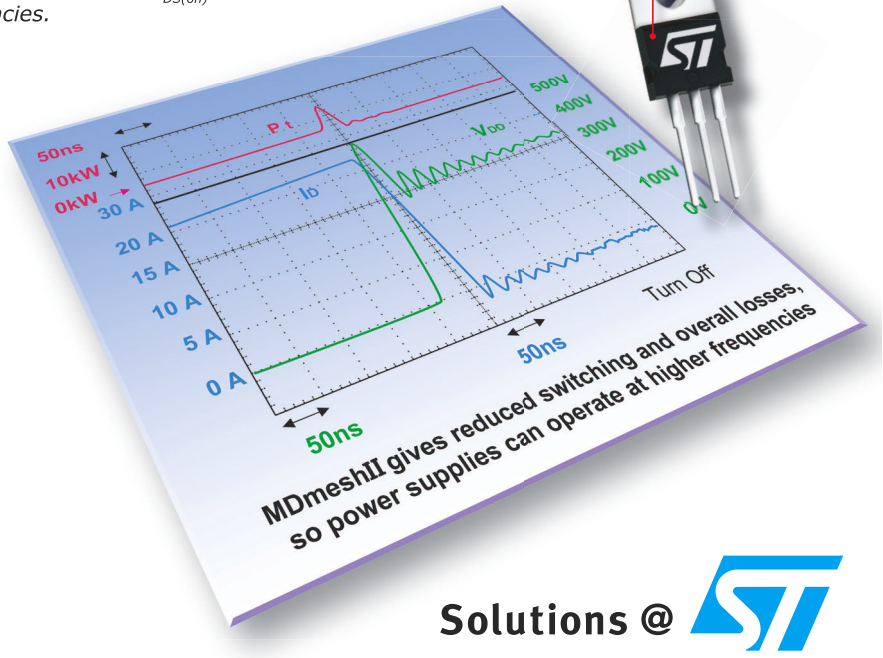
With ST's global solutions offerings such as Power Management ICs, Switching and Low Drop Regulator ICs and a wide range of advanced discrete devices, designing an SMPS for your application is easier than ever. The STP25NM60N using ST's unique MDmeshII™ technology, for example, offers one of the industry's lowest $R_{DS(on)}$ and new levels of performance at high frequencies.

Key Features

- Up to 40% on-resistance reduction
- Typical $R_{DS(on)}$ = 0.140Ω
- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Part Number	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D	Pkge.
STB25NM60N-1	650V	< 0.170Ω	20A	I²PAK
STF25NM60N	650V	< 0.170Ω	20A*	TO-220FP
STP25NM60N	650V	< 0.170Ω	20A	TO-220
STW25NM60N	650V	< 0.170Ω	20A	TO-247
STB25NM60N	650V	< 0.170Ω	20A	D²PAK

* Limited only by maximum temperature allowed



For datasheets, application notes and more information visit www.st.com/mdmesh

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